Reading 35

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A COMPLETE FM TRANSCEIVER

THIS IS A REVISION READING

The purpose of this reading is consolidation of transmitters and receivers by way of looking at the complete block diagram of a typical (and real) 2 metre amateur transceiver. The block diagram has also been placed in the 'downloads' section of the web site in zipped BMP format. The BMP file of the block diagram is only provided for download if you have any trouble printing this PDF file. You can print a BMP file using Paintbrush or Paint, which comes with every Windows operating system.

Description of the block diagram:

The block diagram is that of an amateur transceiver capable of operation on the 2 metre amateur band. I have not shown buffer stages as they should be assumed.

Though there are two antennas shown in the diagram there is in reality only one, and a **small changeover relay** is used to switch the antenna between the transmitter and the receiver. This transceiver is PLL controlled and the PLL's programmable divider is controlled by a microprocessor. The microprocessor also controls the LCD display and keypad. The operator only has to key in the transmit and receive frequencies on the keypad and the microprocessor will set the programmable divider to the correct value (300-1100) and also take care of displaying the appropriate transmit and receive frequencies. It is common to work through repeaters on the 2 metre band and the 'standard' transmitter/receiver offset is 600 kHz. The offset can be set via the keypad and the microprocessor looks after the rest. Notice first that the receiver section is drawn in 'blue', the transmitter in 'green', and the PLL section is 'orange'. If you only have a black and white printer you may like to colour these sections after printing.

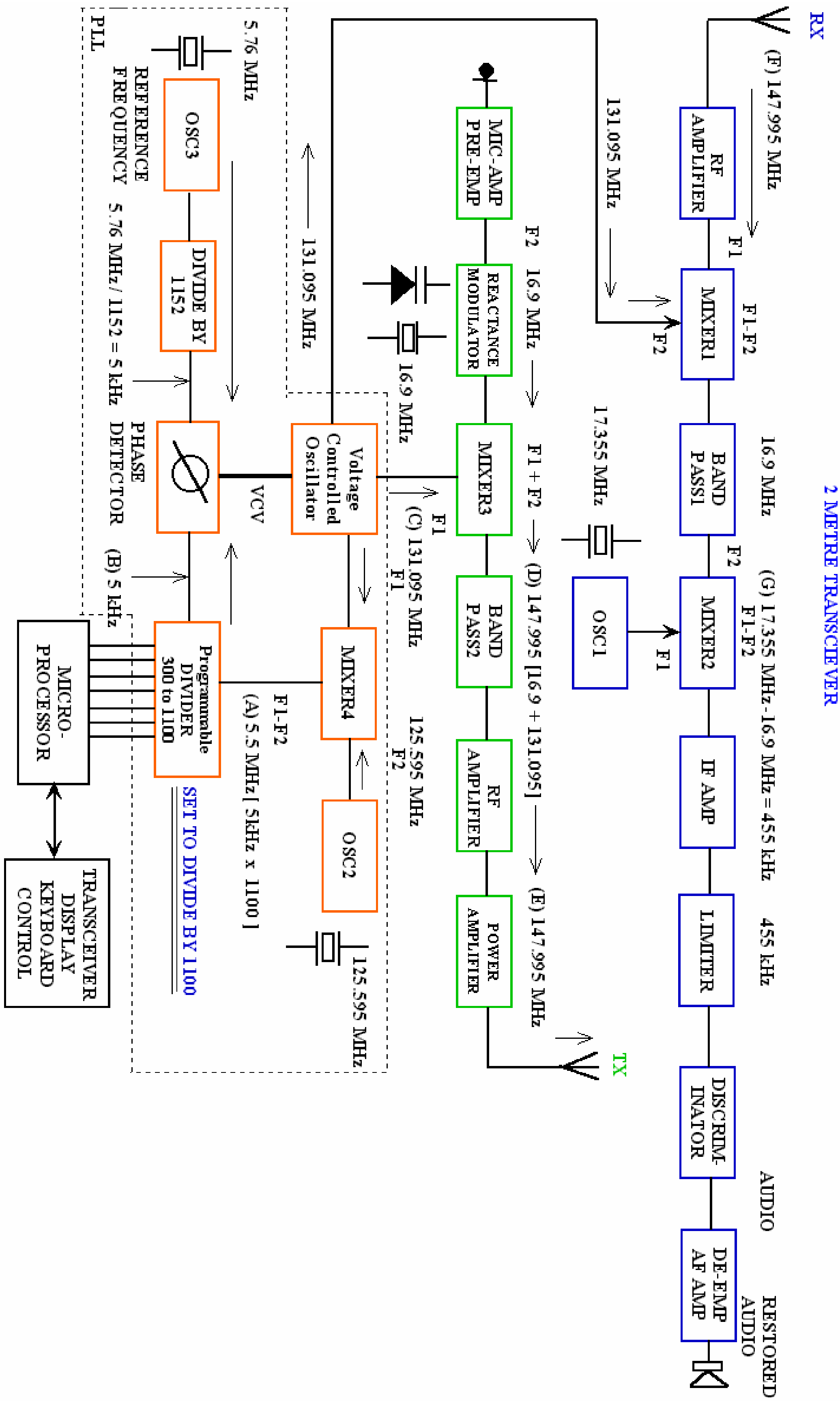
Assume the transceiver is set to transmit and receive on **147.995 MHz.**

This frequency would have been entered on the keypad by the operator and the microprocessor will display the TX and RX frequency on the LCD display as **147.995 MHz. To operate on this (147.995) frequency the microprocessor sets the programmable divider to divide-by-1100.**

The reference oscillator is part of the PLL and provided by OSC3 on 5.76 MHz. This frequency is divided by the fixed divider (divide-by-1152) down to the **reference frequency of 5 kHz.**

The 5 kHz reference frequency signal is fed to the Phase Detector. This means two things:

1. The PLL will be in lock on 5 kHz, and
2. The channel spacing for this radio (the increments between the individual channels) is 5 kHz.


2 METRE TRANSCIEVER
RX
TX
(F) 147.995 MHz
RF AMPLIFIER
F1
MIXER1
F1-F2
F2
131.095 MHz
BAND PASS1
16.9 MHz
MIXER2
F2
F1
(G) 17.355 MHz - 16.9 MHz = 455 kHz
F1-F2
IF AMP
LIMITER
455 kHz
DISCRIM-INATOR
AUDIO
DE-EMP AF AMP
RESTORED AUDIO
OSC1
17.355 MHz
MIC-AMP PRE-EMP
REACTANCE MODULATOR
F2
16.9 MHz
16.9 MHz
MIXER3
F1 + F2
F1
(C) 131.095 MHz
BAND PASS2
(D) 147.995 [16.9 + 131.095]
RF AMPLIFIER
POWER AMPLIFIER
(E) 147.995 MHz
Voltage Controlled Oscillator
VCV
131.095 MHz
F1
MIXER4
125.595 MHz
F2
OSC2
125.595 MHz
F1-F2
(A) 5.5 MHz [5kHz x 1100]
SET TO DIVIDE BY 1100
Programmable DIVIDER 300 to 1100
(B) 5 kHz
PHASE DETECTOR
5.76 MHz / 1152 = 5 kHz
DIVIDE BY 1152
OSC3
5.76 MHz
REFERENCE FREQUENCY
PLL
MICRO-PROCESSOR
TRANSCEIVER DISPLAY KEYBOARD CONTROL

When I say the PLL is in lock on 5 kHz it means that for "lock" to occur the signal coming from the programmable divider is 5 kHz, this is shown on the block diagram as **(B) 5 kHz**. If the signal coming from the programmable divider is not 5kHz then the PLL will not be in lock, and the VCO frequency will change until the PLL comes into lock. The **VCV is the DC control voltage** from the phase detector to the VCO. The VCV voltage will make the **VCO move in frequency very quickly to 131.095 MHz.** When the VCO hits 131.095 MHz the PLL comes into lock, and the VCO is held there.

When the VCO is on 131.095 MHz the PLL will come into lock. As the 131.095 signal is fed from the VCO to MIXER4 along with a signal of **125.595 MHz** from OSC2, this produces a difference frequency F1-F2 of **5.5 MHz** which, when **divided by 1100, equals the reference frequency of 5 kHz, which is fed to the right hand side of the phase detector**.

So, the display says the transmitter and receiver are on 149.995 MHz, and the PLL is producing a very stable signal on 131.095 MHz for use by both the transmitter and the receiver.

TRANSMISSION

The microphone most likely works on the dynamic or capacitor microphone principle. The audio signal from the microphone is **amplified** and **pre-emphasis** is applied. The audio signal is then fed to the **Reactance Modulator** which operates on **16.9 MHz**. Since there is no frequency multiplication in this system, an FM signal with full deviation must leave the reactance modulator (F2). The FM signal F2 is frequency converted to **147.995 MHz** by summing it with the VCO signal F1 in **MIXER3**. The output of MIXER3 also has other unwanted mixing products, and these are eliminated by **BANDPASS2**. The FM signal is then amplified using efficient **Class C** amplifiers and radiated from the antenna.

RECEPTION

The operator releases the **PTT** (push-to-talk) button and the antenna is switched quickly to the receiver circuit. The received FM signal is fed from the antenna to a **wide band RF amplifier,** and then into **MIXER1** where it is mixed with the signal from the VCO on 131.095 MHz. The product F1-F2 of MIXER1 is 16.9 MHz. **BANDPASS1** at the output of MIXER1 eliminates unwanted mixing products from MIXER1. The wanted FM signal (now on 16.9 MHz) is fed to **MIXER2** and frequency converted to the **IF frequency of 455 kHz**.

The 455 kHz FM signal is then highly amplified by the IF amplifier before being fed to the **LIMITER** to remove any amplitude modulation (which would be noise). Upon leaving the LIMITER the FM signal is demodulated by the **DISCRIMINATOR**. The recovered audio from the discriminator undergoes **DE-EMPHASIS** and further audio amplification before being fed to the speaker.

That's it! The full operation of the transceiver in brief. You should now have a good idea how a FM transceiver works and what all the stages do. If you print this diagram you should be able to work out what frequency the transceiver would be operated on if the programmable divider is set to say divide-by-300. I have not shown **ALC** (Automatic Level Control) or **AGC** (Automatic Gain Control), and lines representing these could be drawn onto the diagram. There are a number of options for ALC and AGC.

Other things to think about.

What stage would you adjust to increase or decrease the deviation? I have not done it myself, but it would be a good exercise to look at this block diagram and redraw if for an SSB transceiver on the same band.

As mentioned at the start, this reading is for revision only. In the exam, you will not see anything like the entire block diagram of a transceiver. However, particularly in the AOCP, you may be shown a simplified partial block diagram and be asked to identify the unmarked stage.

If you can understand the block diagram above, and that of an SSB or AM receiver or transmitter, you will certainly have no problems.

You are expected to know the basic operation of a PLL. You will not be asked to do any PLL frequency calculations.

End of Reading 35
Last revision: June 2002

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