

Online Radio & Electronics Course

Supplementary Reading for 27 - Oscillators

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THE BASICS OF PLL FREQUENCY SYNTHESIS

The phase locked loop (PLL) method of frequency synthesis is now the most commonly used method of producing high frequency oscillations in modern communications equipment. There would not be an amateur or commercial transceiver of any worth today that does not employ at least one if not several, phase locked loop systems, to generate stable high frequency oscillations.

PLL circuits are now frequently being used to demodulate FM signals, making obsolete the Foster-Seerly and ratio detectors of early years. Other applications for PLL circuits include AM demodulators, FSK decoders, two-tone decoders and motor speed controls.

The PLL technique has, surprisingly, been around for a long time. In the 1930s the superheterodyne receiver was in its heyday (and it's still going strong today), however attempts were made to simplify the number of tuned stages in the superheterodyne.

THE HOMODYNE RECEIVER

Around 1932, British radio engineers developed a new type of receiver to challenge the 'superhet' - it was called the homodyne or synchrodyne.

The idea was simple: the receiver consisted of a mixer and a local oscillator, followed immediately by an audio amplifier!

When the input signal and local oscillator are mixed at the same phase and frequency, the output is an exact audio representation of the modulated carrier.

Problems, however, occurred in trying to keep the local oscillator on the same phase and frequency as the input signal. To counteract local oscillator drift, the output of the local oscillator was fed together with a sample of the input signal to a phase detector. The output of the phase detector was a correction voltage which was then applied to the local oscillator to keep it on frequency.

It was this type of feedback circuit, which led to the evolution of the phase locked loop. The homodyne receiver was superior to the superheterodyne but the cost of the PLL circuit outweighed its advantages, so the idea did not take off.

In the late 80's some single-chip receivers were developed using the homodyne principle. Such receivers are referred to by some manufacturers as zero intermediate frequency receivers since there is a direct conversion from RF to audio.

DEVELOPING A PLL

Let's have a look at how we can develop our own PLL system, step by step from scratch, and look also at a practical application for the circuit.

About 100 years ago, Pierre Curie along with his brother Jacque, discovered the effect that an electric field has on certain crystals. The Curie's discovered that when physical pressure was applied to certain crystals, electric charges were produced on the opposite faces. Conversely, if an electric field was applied, the crystal structure itself would distort. We know this phenomenon today as the Piezoelectric Effect.

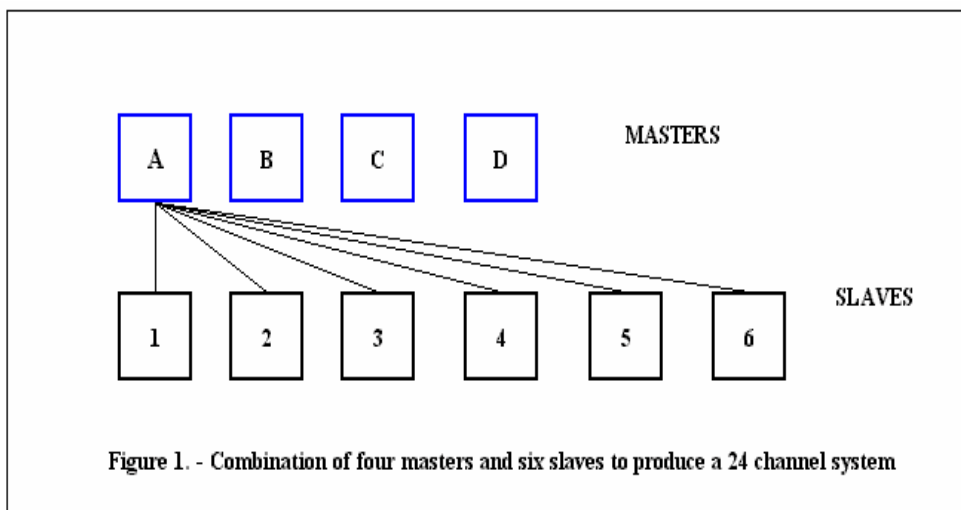
With the invention of 'wireless' there came a need for an accurate frequency-determining device. So evolved the crystal oscillator with its excellent frequency stability.

The crystal oscillator had one major limitation, it could only be used for a narrow range of frequencies. The crystal frequency can only be varied slightly by use of a variable capacitor or the use of circuits designed to respond to harmonics of the crystal's fundamental frequency, as is done with frequency multipliers or overtone oscillators.

For a larger range of frequencies, these methods are not very practical. To obtain a larger frequency range, and maintain essential stability, two crystal oscillators could have their outputs heterodyned (mixed) to produce two new frequencies - ie. the sum and the difference of the two original frequencies.

MASTER / SLAVE

As a practical example: a 24channel system could use four master crystals, heterodyned one at a time with each of six other slave crystals, to give us four times six or 24 output frequencies. See figure 1.



So, with the use of only 10 crystals we can obtain 24 frequencies. This appears OK, but the inhibiting factor in such a system is the cost of the crystals. Imagine the cost of a 400-channel system using crystals!

For those of you who were around at the time of the "illegal" 23 channel CB radio. This master/slave technique was used to generate the 23 channels, though some enterprising "CB operators" worked out they could get an additional channel by switching in the last master/slave combination :-)

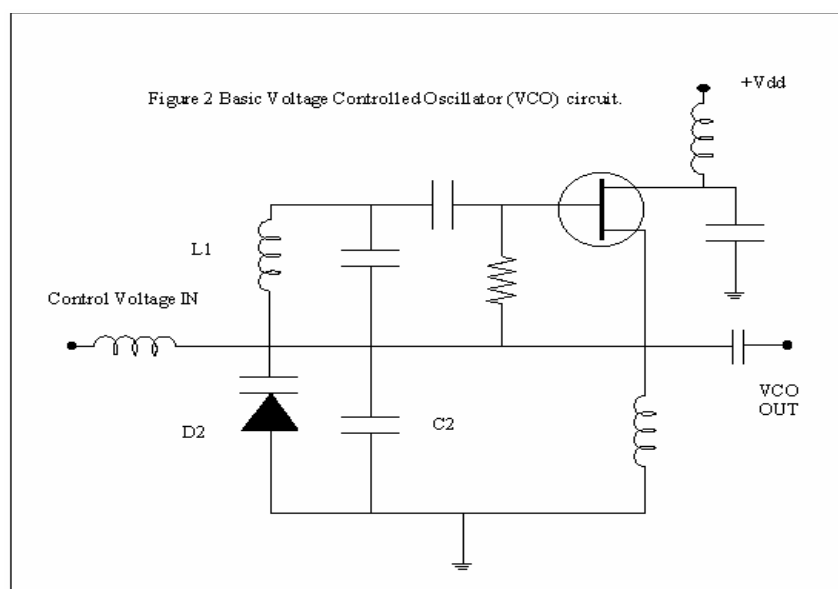
BASIC VOLTAGE CONTROLLED OSCILLATOR

There are oscillators that will operate over a large range of frequencies. Variable frequency oscillators (VFOs) are made to change frequency by changing the value of one of the frequency determining circuits. A voltage-controlled oscillator (VCO) is one in which the frequency-determining component is made to change electrically.

Figure 2 shows a basic voltage controlled oscillator. The frequency of oscillation is determined by L1, C2 and D2. The diode is a varactor, sometimes called a varicap. Most ordinary PN junction diodes will behave as a varicap diode when reverse-biased, but must be operated below the junction breakdown voltage.

With reverse bias, the diode will act as a capacitor, its depletion zone forming the dielectric. Changing the amount of reverse bias within the breakdown limits of the diode will alter the width of the depletion zone and hence vary the effective capacitance presented by the diode. This in turn changes the resonant frequency of the oscillator circuit.

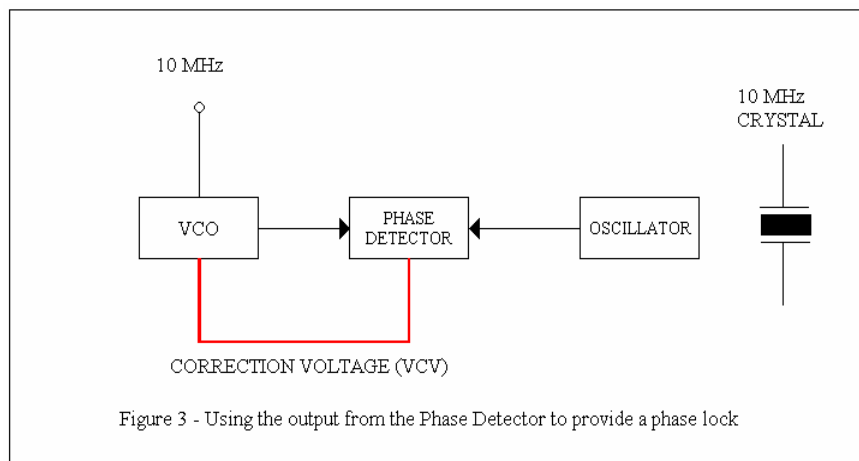
This is all well and good, but how does it help us? After all, the VCO is not stable. Any slight voltage variation in the circuit will cause the frequency to shift. If there was some way we could combine the flexibility of the VCO with the stability of the crystal oscillator; we would have the ideal frequency synthesis system.



Let's try something. Suppose we feed the output of a VCO and a Crystal Oscillator into a phase detector. What's a phase detector? Well it is similar to a discriminator or ratio detector used in frequency demodulation or it could be a digital device (an exclusive-or gate).

If two signals are fed into a phase detector and these signals are equal in phase and frequency, there will be no output from the detector. On the other hand, if the signals are not in phase, the difference is converted to a DC output voltage. The greater the frequency/phase difference in the two signals, the larger the output voltage.

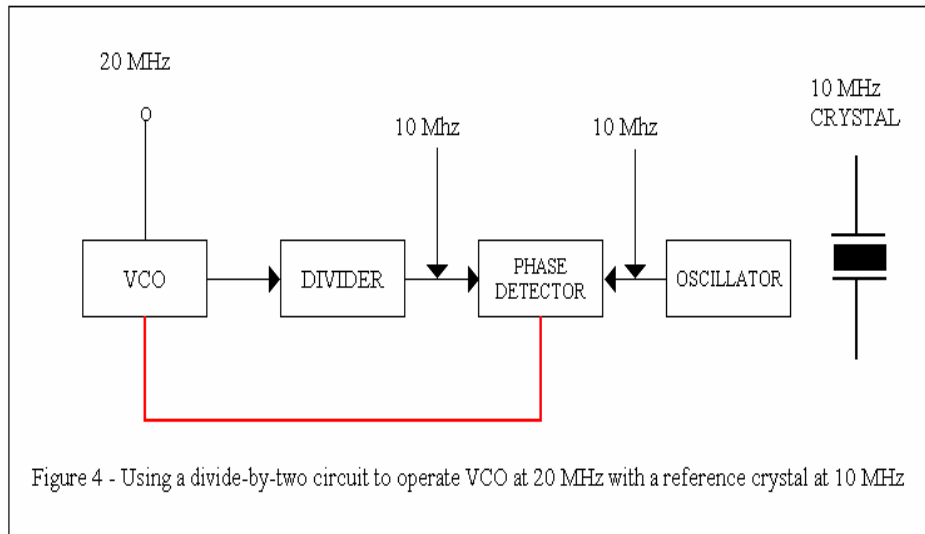
Now, where were we? Right, take a look at Figure 3. The outputs of the VCO and the crystal oscillator are combined with a phase detector and any difference will result in a DC voltage output. Now, suppose this DC voltage is coupled back to the VCO in such a manner that it drives the output of the VCO towards the crystal oscillator frequency - eventually the VCO will LOCK onto the crystal oscillator frequency. This is a PHASE LOCKED LOOP in its most basic form. Only part of the VCO output need be sent to the phase detector. The rest can be usable output.



FURTHER DEVELOPMENT

But wait a minute - the VCO is locked onto the crystal oscillator and is therefore behaving as if it were a fixed frequency oscillator. This gives us the stability of a crystal oscillator, but we have lost the flexibility we were aiming for. We may just as well use the crystal oscillator alone for all the good this arrangement has done us. It certainly doesn't appear as if we have accomplished anything at all.

OK, let's investigate how this problem may be overcome. Suppose our crystal frequency was 10 MHz, but we wanted the VCO to operate on 20 MHz. The phase detector will of course detect a frequency difference and pull the VCO down to 10 MHz, but what if we could fool the phase detector into 'thinking' the VCO was really only operating on 10 MHz, when in reality it is operating on 20 MHz. Take a look at Figure 4.



For example, suppose in Figure 4 we used a divide-by-four instead of the divide-by-two. Then, at lock, the VCO would be oscillating at 40 MHz yet will still be as stable as the crystal reference frequency.

COUNTER/DIVIDERS

If we could design a divider that would enable us to change the ‘divide by’ figure at will, we would certainly have a very versatile frequency generating system.

Such frequency dividers are available, and are known as Programmable Frequency Dividers. The internal operation of such circuits is not within the scope of this article, but let's have a look at the basic principle involved.

Programmable dividers are digital circuits in that they operate with two voltage levels, a low-level (0) and a high level (1). Ordinary circuits which operate on all voltages are called ANALOG. As the VCO is an analogue device, the sine waves it outputs to the frequency divider needs to be converted into square waves - changing the wave shape, but not the frequency.

The divider is really a pulse counter. It can be programmed to count to two and then reset, count to two again and reset, and so on. At each reset, one pulse is output from the divider - this is a divide-by-two action. This divider would be suitable for our circuit of Figure 4.

More elaborate counter/dividers can be designed to count to different amounts before resetting - eg., a count-to-four divider would be a divide-by-four; a count-to-35 would be a divide-by-35; and so on. Remember that no matter what the reset level is, we only get one output pulse from each reset. The counter/divider may have several inputs which can be programmed in binary or some other digital code to determine its divide-by number. For example, if the divider had four inputs to be coded in binary, and we applied a high level on inputs 1 and 3, a binary code of 1010 (which is the equivalent of decimal 10), we would

have a divide-by-10 action. More specialised programmable dividers provide for a large range of frequency divisions.

A VERSATILE PLL

Now we have assembled all the necessary components for a workable PLL system: a Voltage Controlled Oscillator, a Crystal Oscillator, a Programmable Divider and a Phase Detector.

One of the most versatile PLL systems, seen particularly in Citizens Band receivers, is the UNIDEN 858. Figure 5 shows a block diagram of the system. Let's work through it step by step and see what we can discover.

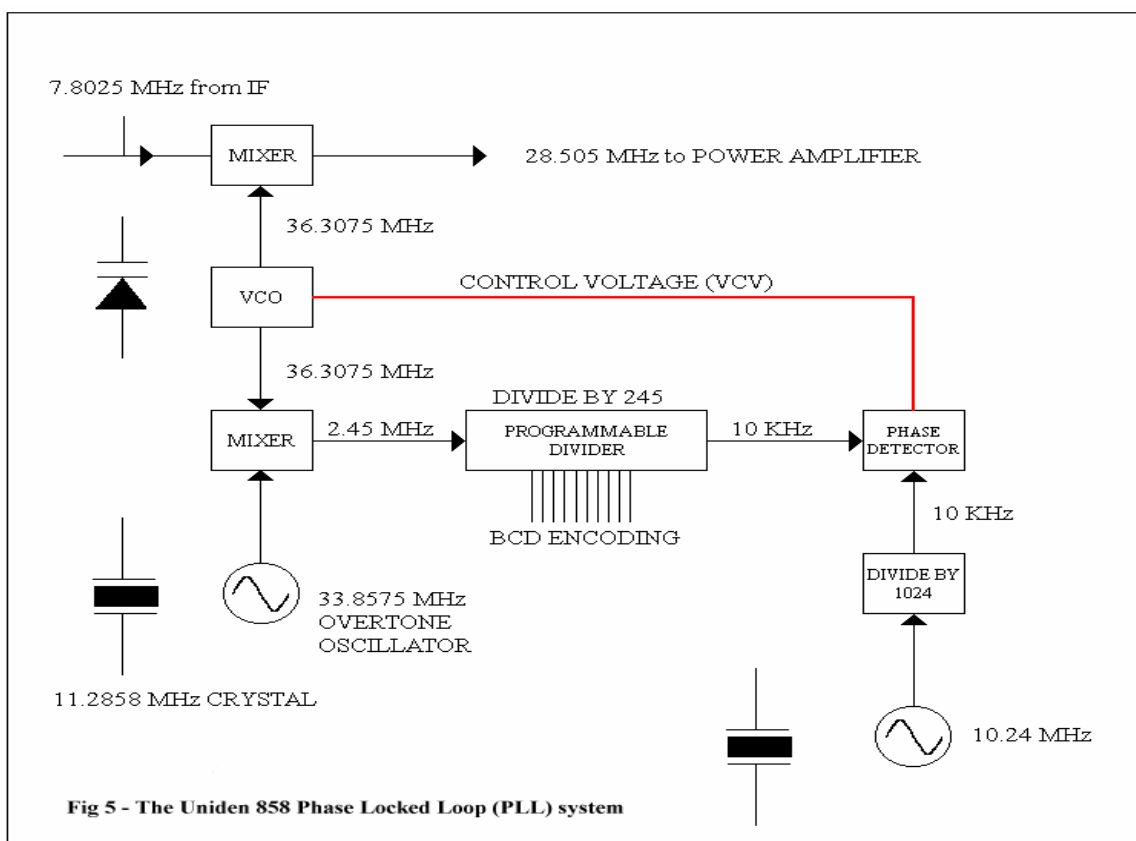


Fig 5 - The Uniden 858 Phase Locked Loop (PLL) system

The reference crystal in this case is 10.24 MHz, but note that in this instance the reference crystal is not oscillating at the reference frequency - its signal is passed through a 1024 divider to give us a reference frequency of 10 kHz. This 10 kHz reference signal is passed to the phase detector.

Now we know that the signal coming from the VCO must be divided to 10 kHz before being applied to the phase detector - but notice one thing: in this system our VCO must oscillate at around 36 MHz to give us the correct output frequency. This frequency is going to take a lot of dividing to get it down to the 10 kHz reference frequency.

So here a cunning method has been used to convert the VCO frequency to a workable value before division. This is where the 11.2858 MHz crystal oscillator comes into play. It's an overtone oscillator producing an output on the third overtone of the crystal's fundamental frequency - ie. 33.8575 MHz. This signal is then mixed with the VCO output, the difference frequency being around 2 to 3 MHz. This signal can then be divided to 10 kHz quite simply and applied to the phase detector.

Before we get too involved in some actual circuit frequencies, let's look more closely at the frequency divider.

We see that it is a programmable divider; it can be set to divide by any amount from 1 to 399. The input data to the divider is binary coded decimal (BCD) and is applied to pins 13 through 22 on the actual integrated circuit.

What's BCD? It's a method of expressing a decimal value as a four-bit binary number. The units in the decimal number are expressed as a four-bit binary number, as are the tens, then the hundreds, etc. For example, decimal 251 would require three four-bit conversions: 1 is expressed as 0001; 5 becomes 0101; and 2 equals 0010. The final figure is the chain of the three four-bit numbers: 251 equals 0010 0101 0001 in BCD.

The divider has 10 inputs. These inputs can be set with a BCD code in the range 0 to 399 which equates to 400 channels. For channel 399 the four bit BCD code would be 0011-1001-1001 (3-9-9).

So there are a total of 400 possible input combinations to the programmable divider, which theoretically means 400 operating frequencies, provided the radio frequency stages of the transceiver remain in tune or are tuned accordingly.

A logic (1) is represented by a +5V input level and a logic (0) by zero volts. If the input to the divider is supplied with the BCD code for 146 (0001 0100 0110) then the input signal will appear at the output divided by 146.

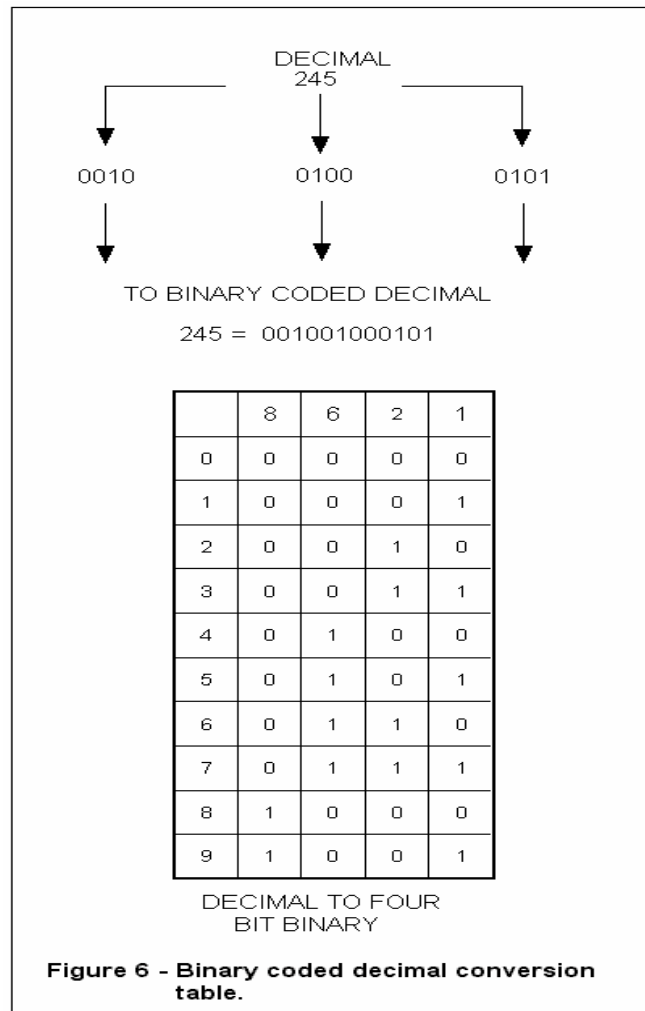
Another point worth mentioning is that the VCO signal is not the final transmit frequency. All necessary processing of the signal to be transmitted is performed before the PLL stage is reached. The output of the VCO is then mixed with the intermediate frequency (IF) and the difference frequency produced is the actual transmit frequency.

Conversely, during receive operation, the VCO and the incoming signal are heterodyned to produce the IF frequency.

A WORKED EXAMPLE

Let's take a desired output of 28.505 MHz, and develop the conditions which would need to exist around the circuit. Since the output is 28.505 MHz, the VCO will be 7.8025 MHz higher (the IF frequency). The VCO is therefore 36.3075 MHz. This is fed to the mixer along with a 33.8575 MHz signal derived from the third overtone of the 11.2858 MHz crystal oscillator.

The 36.3075 MHz and 33.8575 MHz signals mix to produce a difference frequency of 2.45 MHz. Now the divider must be set to divide the 2.45 MHz frequency down to 10 kHz. This requires a BCD code on the data inputs equivalent to 245 decimal (divide-by 245). The logic levels applied to the 10 BCD inputs would be 10 0100 0101

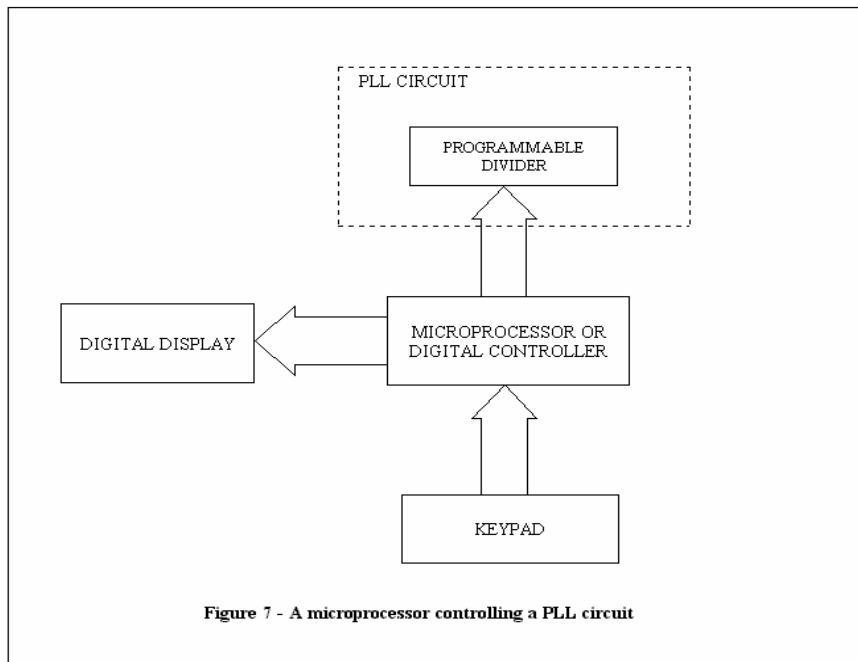


The 10 kHz signal produced by the divider is phase detected with the stable 10 kHz reference frequency from the crystal oscillator and a control voltage applied back to the VCO. After a very brief period the circuit will establish lock.

Changing the divide-by number will change the output frequency in 10 kHz steps over a maximum frequency range of $400 \times 10 \text{ kHz} = 4 \text{ MHz}$. Incrementing or decrementing the divider will alter the VCO frequency by 10 kHz. So the channel spacing in this case is 10 kHz.

If you think there is some relationship between the 10 kHz reference frequency and the 10 kHz channel steps, then you're right! If 5 kHz channel spacing was required, all that would be necessary is to change the 1024 divider to a 2048 divider. The 858 chip has provision on board for this - pin 7 can be toggled between high and low to change from 1024 to 2048.

A microprocessor can be added to the PLL circuit to control the logic fed to the programmable divider. Such systems are common in modern communications receivers/transmitters. See figure 7. Now a whole new scope of functionality is available. The microprocessor can be told what to do from a keypad - and its internal program can do things like change frequency, memorise frequencies, scan a range of frequencies, or operate between different programmable transmit and receive frequencies, and much more. The microprocessor can even re-tune the VCO and other parts of the transceiver to give extremely broadband coverage. An alternative to re-tuning the VCO is to have several VCO's and have the microprocessor switch the appropriate one into circuit for the desired frequency range.



You now should have a very good idea of the way PLL frequency synthesis systems work. More complex systems do exist but they are merely extensions of what has been described. Some modern communications equipment may use not one, but several PLL's, and even PLL's within PLL's.

If you want to learn more experiment with an old CB Radio.

End of Reading – Supplementary 27.

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