

SN54LS112A, SN54S112, SN74LS112A, SN74S112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

D2661, APRIL 1982—REVISED MARCH 1988

SDLS011

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset and clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54LS112A and SN54S112 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS112A and SN74S112A are characterized for operation from 0°C to 70°C .

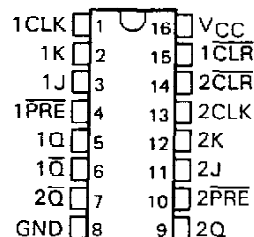
FUNCTION TABLE (each flip-flop)

| INPUTS | | | | | OUTPUTS | |
|--------|-----|-----|---|---|----------------|----------------|
| PRE | CLR | CLK | J | K | Q | \bar{Q} |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H [†] | H [†] |
| H | H | ↓ | L | L | Q ₀ | \bar{Q}_0 |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | TOGGLE | TOGGLE |
| H | H | H | X | X | Q ₀ | \bar{Q}_0 |

[†] The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} minimum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

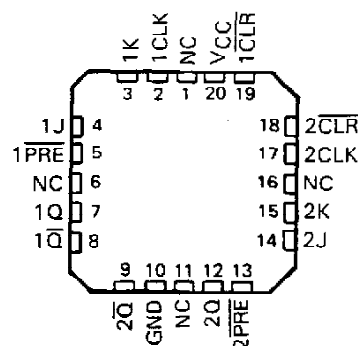
SN54LS112A, SN54S112 . . . J OR W PACKAGE
SN74LS112A, SN74S112A . . . D OR N PACKAGE

(TOP VIEW)



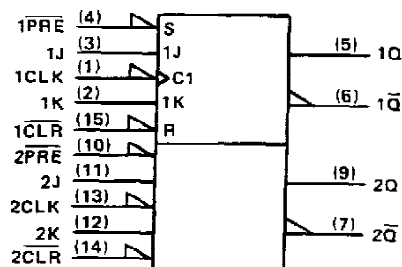
SN54LS112A, SN54S112 . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

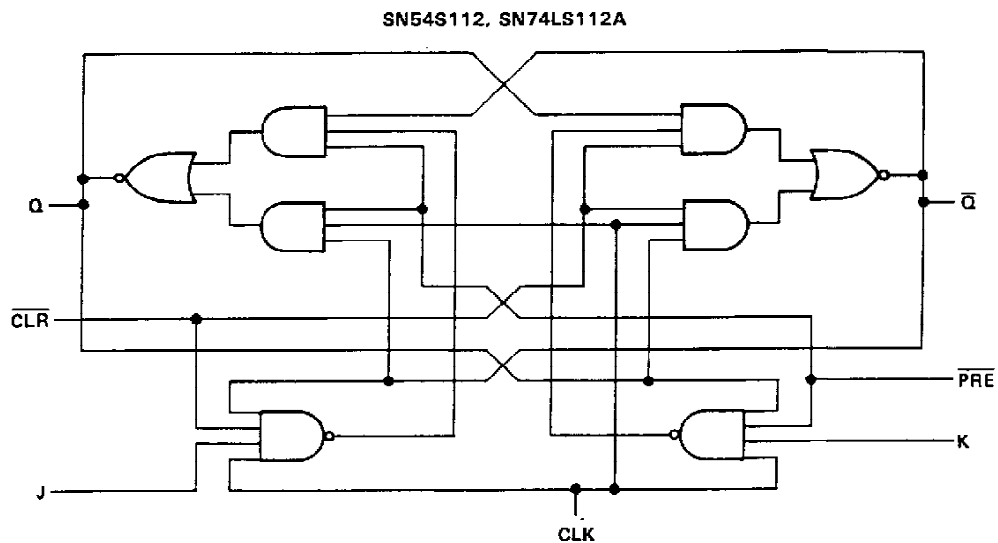
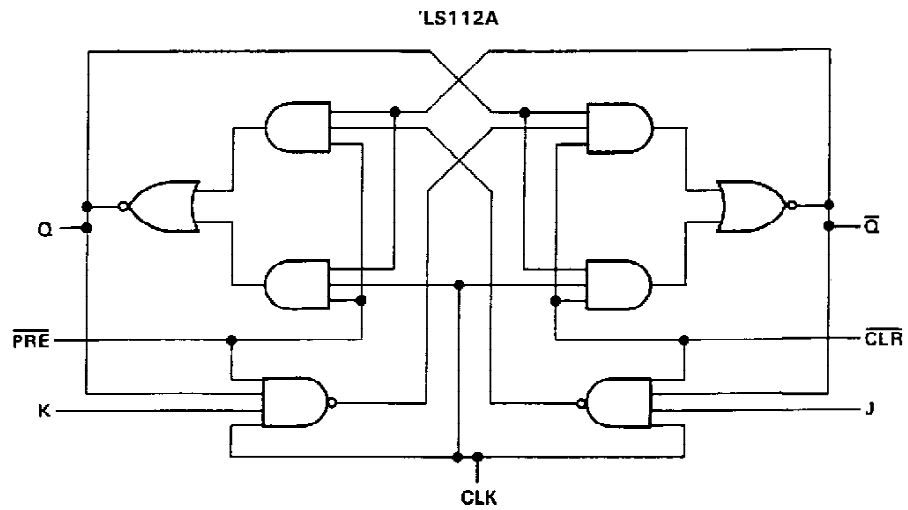
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logic diagrams (positive logic)



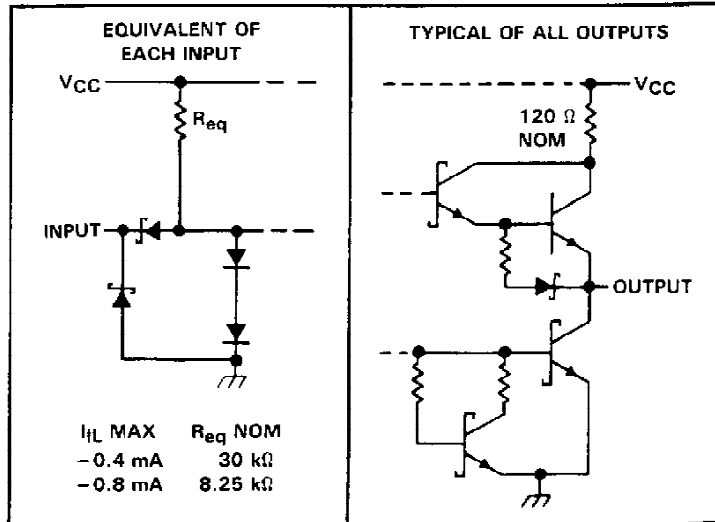
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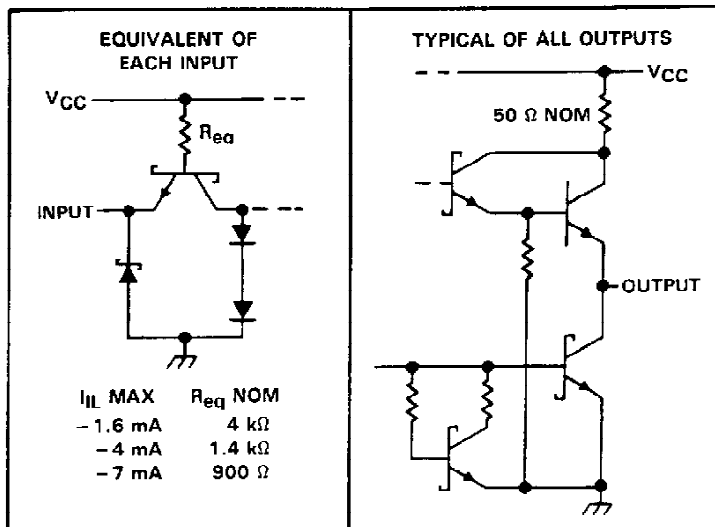
SN54LS112A, SN54S112, SN74LS112A, SN74S112A
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET AND CLEAR

schematics of inputs and outputs

'LS112A



SN54S112, SN74S112A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage: 'LS112A | 7 V |
| SN54LS112, SN74LS112A | 5.5 V |
| Operating free-air temperature range: SN54' | -55°C to 125°C |
| SN74' | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

SN54LS112A, SN74LS112A

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

| | | SN54LS112A | | | SN74LS112A | | | UNIT |
|-------------|--------------------------------|------------------|-----|------|------------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.7 | | | 0.8 | V |
| I_{OH} | High-level output current | | | -0.4 | | | -0.4 | mA |
| I_{OL} | Low-level output current | | | 4 | | | 8 | mA |
| f_{clock} | Clock frequency | 0 | | 30 | 0 | | 30 | MHz |
| t_w | Pulse duration | CLK high | | 20 | | 20 | | ns |
| | | PRE or CLR low | | 25 | | 25 | | |
| t_{su} | Set up time-before CLK↓ | Data high or low | | 20 | | 20 | | ns |
| | | CLR inactive | | 25 | | 25 | | |
| | | PRE inactive | | 20 | | 20 | | |
| t_h | Hold time-data after CLK↓ | 0 | | | 0 | | | ns |
| T_A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN54LS112A | | | SN74LS112A | | | UNIT |
|------------------|------------|--|------------|------|------|------------|------|------|---------------|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{IK} | | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$ | | | -1.5 | | | -1.5 | V |
| V_{OH} | | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$ | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| V_{OL} | | $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$ | 0.25 | 0.4 | | 0.25 | 0.4 | | V |
| | | $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$ | | | | 0.35 | 0.5 | | |
| I_I | J or K | $V_{CC} = \text{MAX}, V_I = 7 \text{ V}$ | | | 0.1 | | | 0.1 | mA |
| | CLR or PRE | | | | 0.3 | | 0.3 | | |
| | CLK | | | | 0.4 | | 0.4 | | |
| I_{IH} | J or K | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$ | | | 20 | | | 20 | μA |
| | CLR or PRE | | | | 60 | | 60 | | |
| | CLK | | | | 80 | | 80 | | |
| I_{IL} | J or K | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$ | | | -0.4 | | | -0.4 | mA |
| | All other | | | | -0.8 | | -0.8 | | |
| I_{OS}^{\S} | | $V_{CC} = \text{MAX},$ see Note 2 | -20 | | -100 | -20 | | -100 | mA |
| I_{CC} (Total) | | $V_{CC} = \text{MAX},$ see Note 3 | | 4 | 6 | | 4 | 6 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTES: 2. For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with $V_O = 2.25 \text{ V}$ and 2.125 V for the '54 family and the '74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

3. With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

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FLIP-FLOPS WITH PRESET AND CLEAR

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|-----------|--|----------------------------|---|-----|-----|-----|------|----|
| f_{max} | | | $R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$ | 30 | 45 | | MHz | |
| t_{PLH} | $\overline{\text{CLR}}$, $\overline{\text{PRE}}$ or CLK | Q or $\overline{\text{Q}}$ | | | 15 | 20 | | ns |
| t_{PHL} | | | | | 15 | 20 | | ns |

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

SN54S112, SN74S112A
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

| | | SN54S112 | | | SN74S112A | | | UNIT |
|-----------------|--------------------------------|------------------|-----|-----|-----------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} | Low-level input voltage | 0.8 | | | 0.8 | | | V |
| I _{OH} | High-level output current | -1 | | | -1 | | | mA |
| I _{OL} | Low-level output current | 20 | | | 20 | | | mA |
| t _w | Pulse duration | CLK high | | 6 | 6 | | ns | |
| | | CLK low | | 6.5 | 6.5 | | | |
| | | PRE or CLR low | | 8 | 8 | | | |
| t _{su} | Set up time-before CLK↓ | Data high or low | | 7 | 7 | | ns | |
| t _h | Hold time-data after CLK↓ | 0 | | | 0 | | | ns |
| T _A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN54S112 | | | SN74S112A | | | UNIT |
|-------------------|-----------|--|----------|------|-------|-----------|------|-----|------|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V _{IK} | | V _{CC} = MIN, I _I = -18 mA | -1.2 | | | -1.2 | | | V |
| V _{OH} | | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -1 mA | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| V _{OL} | | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA | 0.5 | | | 0.5 | | | V |
| I _I | | V _{CC} = MAX, V _I = 5.5 V | 1 | | | 1 | | | mA |
| I _{IH} | J or K | V _{CC} = MAX, V _I = 2.7 V | 50 | | | 50 | | | μA |
| | All other | | 100 | | | 100 | | | |
| I _{IL} | J or K | V _{CC} = MAX, V _I = 0.5 V | -1.6 | | | -1.6 | | | mA |
| | CLR‡ | | -7 | | | -7 | | | |
| | PRE‡ | | -7 | | | -7 | | | |
| | CLK | | -4 | | | -4 | | | |
| I _{OS} † | | V _{CC} = MAX | -40 | -100 | | -40 | -100 | mA | |
| I _{CC} # | | V _{CC} = MAX, see Note 3 | 15 25 | | 15 25 | | | mA | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Clear is tested with preset high and preset is tested with clear high.

¶ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

Values are average per flip-flop.

NOTE 3: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.



SN54S112, SN74S112A
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET AND CLEAR

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|-----------------------|--|-----|-----|-----|------|
| f_{max} | | | $R_L = 280\ \Omega, \quad C_L = 15\ \text{pF}$ | 80 | 125 | | MHz |
| t_{PLH} | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or \overline{Q} | | | 4 | 7 | ns |
| t_{PHL} | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ (CLK high) | \overline{Q} or Q | | | 5 | 7 | ns |
| | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ (CLK low) | | | | 5 | 7 | |
| t_{PLH} | CLK | Q or \overline{Q} | | | 4 | 7 | ns |
| t_{PHL} | | | | | 5 | 7 | ns |

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

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