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Motorola Advanced Amplifier Concept Package

Prepared by: Alan Wood
Motorola Semiconductor Products Sector

ABSTRACT

This paper describes the philosophy and the design of a new generation of RF power transistors which, for Land Mobile products, offer a unique design concept that will simplify the external matching requirements for high power 800 MHz amplifiers. An additional benefit is the increased efficiency that can be obtained over a wider bandwidth. These improvements are brought about by the use of multiple matching sections inside the package. Presented here will be an analysis of the design of a doubly input/output matched part showing its advantages over a conventionally matched 800 MHz transistor. Also described will be the performance characteristics of two RF devices, soon to be introduced by Motorola Semiconductor Products Sector. They will be rated at 60 watts output power for application in mobile radio–telephones (12 V operation) and base stations (24 V), specifically cellular, trunked and conventional 800 MHz systems.

INTRODUCTION

In a number of RF transmitter applications in the 800 to 960 MHz band, e.g. paging and cellular base stations and high power mobiles it is not uncommon for the amplifier output stage to have multiple devices in parallel. RF circuit designers would prefer to replace these complex multi device stages with a single device or at least with fewer paralleled transistors. But increasing the output power of current 800 MHz transistors does present a number of problems: larger transistor die would lower the manufacturing yields, dissipating the additional heat in the existing package would limit the maximum operating temperatures, and the device impedances would be so low that broadband amplifier design would be extremely difficult.

High power RF transistors developed for these applications must therefore exhibit a number of desirable features namely:

i. Power Gain. Gain should be as high as achievable using the current processing technology but not at the neglect of other important parameters, i.e. ruggedness and stability.

ii. Power Added Efficiency. High efficiency is of paramount importance in any high power amplifier application. Space requirements limit the volume that can be dedicated to power supplies and heatsinking structures. Invariably this results in a less efficient device operating at higher junction temperatures and consequently lower reliability.

iii. Low Thermal Resistance. Higher output power ratings correspond to higher concentrations of heat in a RF transistor. This is to some degree offset by a larger die size but doubling the output power, assuming similar efficiency, will double the heat dissipation in the package. Making the package larger will not necessarily decrease the thermal resistance and will certainly compromise the performance by increasing the package parasitics.

iv. Bandwidth. Current transmitter power amplifier designs strive to cover the full allowable operating bandwidth for their own particular application. The benefits of lower inventory and the elimination of field tuning over split band designs outweigh the added complexity in the design and the trade–offs in performance over narrow–band tuning.

v. Stability. An amplifier should be stable over the full operating range expected in the field.

vi. Load–Pull Ruggedness. A transistor should be capable of surviving an output mismatch even when operating at the design extremes. To achieve this degree of ruggedness does involve trade–offs in both gain and efficiency.

vii. Consistent Performance. Performance and device characteristics need to be consistent not only part to part but also batch to batch if they are to be usable by any equipment manufacturer. Inconsistency will make it difficult for the product development engineer to guarantee the final performance of his design and eventually it will lead to excessive guard–banding in the component specifications. Lower product yields when testing to a more stringent specification inevitably results in higher component cost.

Most of the above attributes are determined by the die performance and the inter–relationship of the die and the package. At higher frequencies, UHF and above, the package interface with the external circuit also becomes important. Device impedances are relatively low compared with the 50 ohm terminating impedances of an amplifier. For this reason minor variations in package position, grounding, and the values of external components can have a significant influence on the amplifier performance. In fact even minor variations in the position of the input/output shunt capacitors can easily cause an amplifier to exhibit lackluster performance.

Incorporating more of the impedance transformation network inside the package minimizes the effects of these variations and simplifies the task of the circuit designer. As an added benefit it makes the out–going RF testing by the transistor manufacturer easier, since it simplifies test fixture design and maintenance.

DIE CONSIDERATIONS

RF transistor die design is a compromise between obtaining the best performance possible in terms of power gain, saturated output power and efficiency, while still maintaining adequate ruggedness into an output mismatch, good voltage breakdowns and long term reliability. Good die yields and low production costs are also important in developing transistor die for use in Land Mobile applications.

MATCHING NETWORKS

Figure 1 is a very simplified T model of a transistor die in common base configuration. Common base is normally chosen instead of common emitter mode for class C amplifiers operating at 800 MHz and above because of its higher power gain. Included in the model are the junction capacitances and the resistive losses attributed to each transistor region. The values given are typical for a 60 watt die designed for operation at 12.5 Volts.

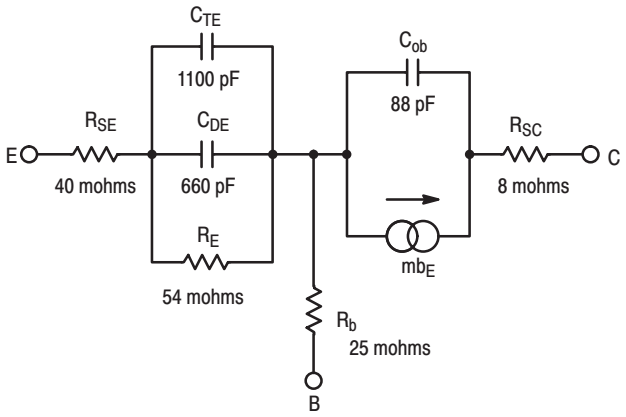

Figure 1. Simplified 'T' Model for Transistor Die

Analysis of this model at 870 MHz gives us the equivalent series input impedance (Z_{in}) and the equivalent series output impedance, (Z_{OL}), that when matched by a conjugate impedance source and load will operate at the rated output power level with minimum reflected power.

$$Z_{in} = 0.105 - j0.022 \text{ Ohms}$$

$$Z_{OL} = 0.717 - j0.38 \text{ Ohms}$$

Inspection of the series impedances given above indicates bandwidth is not inherently limited by the die below the cut–off frequency (ft). The series output impedance has the highest Q but even for this large die it is still less than one.

RF power transistors are not generally sold in chip form but are normally assembled in packages or chip carriers before they can be usefully incorporated in discrete amplifier circuits. The package provides low resistive paths for both thermal and electrical connections. It should also provide a method of mechanically attaching the device to a heatsink. Electrical connections inside the package at high frequencies have a marked effect on the performance of the transistor. Figure 2 includes these package parasitics in the transistor model. For our purposes this model can be simplified to that given in Figure 3. The values given are typical for a non–internally matched 800 MHz package.

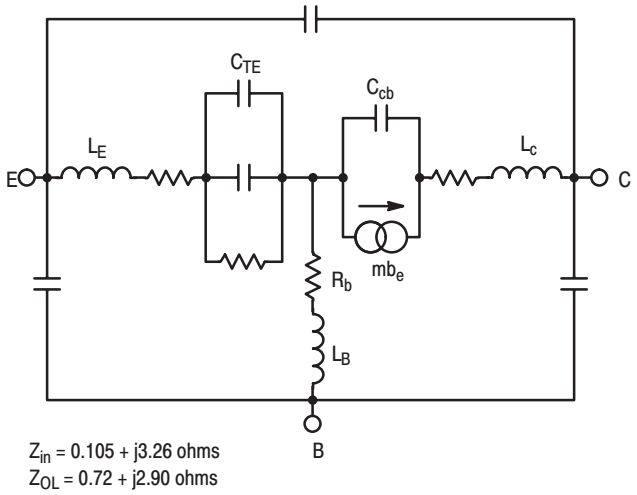

Figure 2. Model for Un–Matched Packaged Die

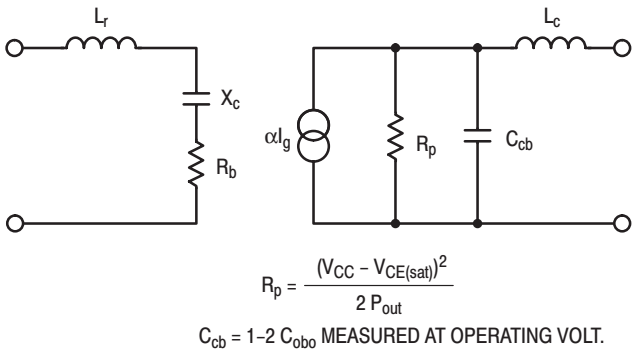

Figure 3. Device Equivalent Model

Analysis of this model gives the impedances at the package terminations to be:

$$Z_{in} = 0.105 + j3.258 \text{ Ohms}$$

$$Z_{OL} = 0.717 + j2.90 \text{ Ohms}$$

These are very low impedance levels compared to the 50 ohm termination impedances of an amplifier and impedance transforming networks are essential if an amplifier is to meet its design goals. Without these networks the amplifier would exhibit:

* Poor input return loss. A large part of the drive will be reflected and thus not available for amplification by the transistor.
* Poor gain flatness and consequently limited bandwidth.
* Poor transfer of power to the load because of output mismatch.
* Instability under certain operating conditions.

Matching networks can be implemented externally but the package parasitic components will severely limit the useful bandwidth on high power devices. The inevitable losses associated with these external components and the sensitivity of the amplifier performance to component variation will also reduce the attainable bandwidth in production designs. The inherent narrow bandwidth of a packaged transistor die at high frequencies was partly solved several years ago by including part of the input network inside the package. Later further improvements were made, especially in the case of microwave power devices, by including additional sections of input matching and output

matching within the device package. The added complexity of multi–section internal matching requires the use of highly skilled labor and careful attention to detail in the assembly of these transistors. Even with these measures the product yields are relatively low compared to commercial products and consequently these parts are expensive to manufacture.

Input Network

Internal input matching performs two functions. It increases the impedances to a level that can be more readily matched by external components. Secondly, using the internal feedback inherent in the package, internal matching can be used to shape the gain–frequency response of the device. The feedback is associated with the common lead inductance and in either CE or CB configurations there will always be a small amount of common lead inductance simply due to the physical distance between the die and the grounded leads. This inductance is represented by the emitter or base die metallization, the wire–bonds from the bond pads to the lead frame and the lead–frame itself. The inductance is minimized by having several wire bonds to the die, using wide metallization patterns on the package and having two or more common leads — four is normal. This is illustrated in Figure 4.

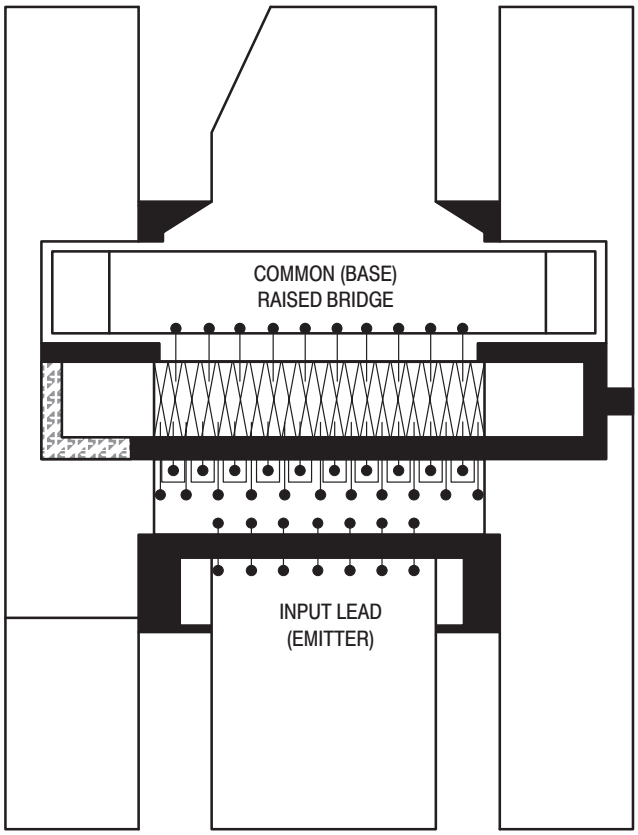

Figure 4. Internal Layout of Current 800 MHz Package

The self and mutual coupling that exists in a double wire bonded common base or common emitter part can be tuned to vary the gain of the transistor at a particular frequency. Using this method the 6 dB gain slope per octave for the die can be flattened over a desired frequency range.

The input impedance without matching was given earlier and is repeated here:

$$Z_{in} = 0.105 + j3.258 \text{ Ohms}$$

Wirebond inductance and the braze area, necessary for lead attach, are responsible for the major part of the reactive component. Using current packaging techniques it would be difficult to further minimize this inductive component.

A matter of considerable importance is, however, the bandwidth over which the transistor can be operated without serious degradation in power gain and efficiency. The high Q represented by this impedance would present an insurmountable difficulty for any engineer wishing to design even a moderately broadband circuit. Additionally the high losses associated with the shunt capacitor necessary to transform the inductive reactance would severely degrade amplifier performance. This can be demonstrated using the values given in equation above. The unmatched device Q would be:

$$Q = X_S/R_S \quad (1)$$
$$= 3.258/0.105 = 31$$

Typical Qs for high quality chip capacitors at this frequency are in the range 100–300. This represents a gain decrease due to losses in the capacitor of between 0.9 dB and 3 dB. Typical gains for parts operating at 12.5 Volts are 5–6 dB so this does represent a significant factor in circuit performance.

The series inductance internal to the package also limits the bandwidth that can be achieved with external input matching. Figure 5 is a plot of the frequency versus input VSWR of the input network shown in Figure 6. This analysis assumes ideal loss–less components. The inductive reactance of the device input impedance is resonated with a single shunt capacitor at the band center. This gives the 3 dB bandwidth from:

$$BW\ (3\ dB) = \frac{f_o}{Q} = \frac{f_o\ R_S}{X_S} \quad (2)$$
$$= \frac{870 \times 10^6 \times 0.105}{3.258}$$
$$= 28 \text{ MHz}$$

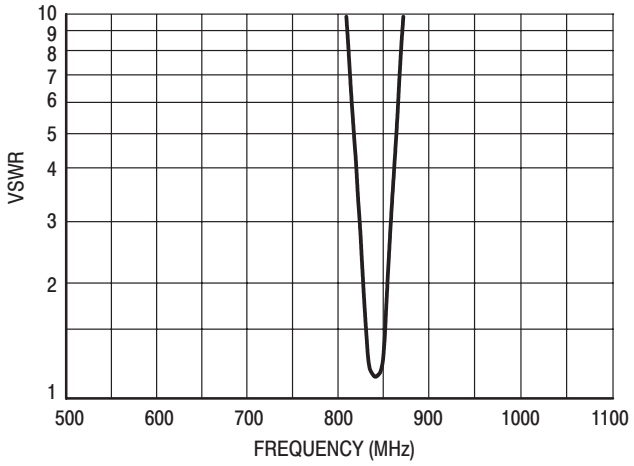

Figure 5. Bandwidth for Non–Internally Matched Input

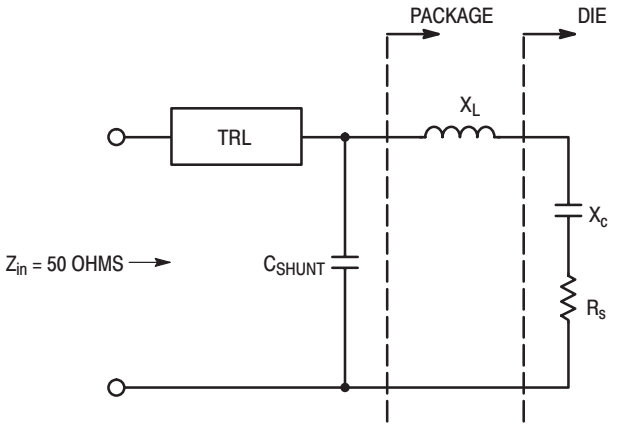

Figure 6. Input Network for Unmatched Transistor

The real part of the series equivalent input impedance, R_S, is inversely proportional to the area of the transistor, or more exactly the emitter periphery, which itself determines the saturated output power. This explains why low power transistors can easily be matched over several hundreds of megahertz whereas high power devices have limited bandwidth. The 3 dB bandwidth given in equation 2 is the theoretical maximum that can be achieved. Fano, in his classic paper (1), analyzed the limitations of broadband matching a complex load. His work asserts that increasing the number of sections does allow the 3 dB bandwidth to be transformed into a nearly rectangular bandpass characteristic but no matter how complicated the network, it is never possible to match the entire available drive over a wider frequency band.

Radical improvements in bandwidth can be achieved if the series inductance is split by including a single stage of matching inside the package. Bandpass networks offer better performance than low–pass configurations using the same number of elements but low–pass impedance transforming structures have a topology that can be easily integrated internally using the wirebonds for inductors and MOS–capacitors for the shunt elements. MOS–capacitors can be fabricated using the same technology employed in the manufacture of transistor die and offer very low dissipation at UHF frequencies.

An alternative matching structure has been proposed (2) using a shunt–L element, inside the package, to resonate with the die input capacitance at mid–band. There are some reported advantages with this scheme namely, higher power gain, and improved collector efficiency. The shunt–L network also results in a band–pass structure with effectively zero reactance at low frequencies. This suppresses the generation of low frequency instabilities. A major disadvantage of this matching scheme is the inability to screen the assembled device for certain dc parameters.

Figure 7 illustrates the advantages of internal matching comparing an un–matched package with a package incorporating a single section. The input impedance measured at the device terminals is still relatively low but it is now practical to transform it to a higher impedance externally.

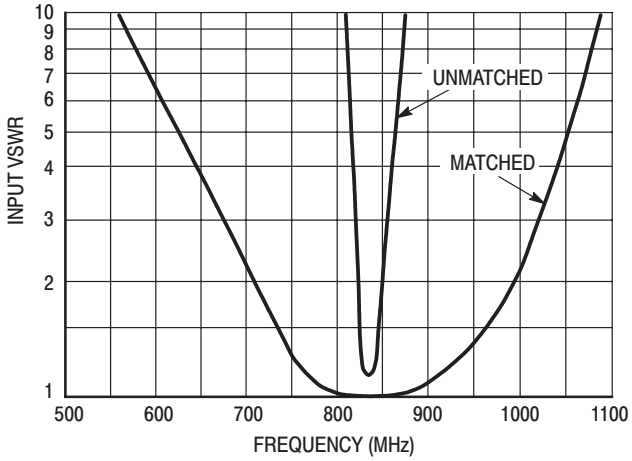

Figure 7. Bandwidth for Internally Matched Input

A further improvement in the input impedance can be achieved by adding more sections of input matching. Matthaei has covered in depth the design of low–pass impedance transforming networks ideally suitable for this application (6). With two sections up to 90% of the input power can be matched over the available bandwidth. Figure 8 illustrates the behavior of the double input matched device with frequency. Input impedance is now at a level where the external matching can be readily accomplished using a single section transmission line transformation Figure 9.

Additional bandwidth can be obtained and the gain frequency response flattened by mismatching the input at the low frequency end of the band. The 6 dB/octave gain slope of the transistor die can be used to advantage to extend the low frequency response. A less than perfect input match partially reflecting the input power is compensated for by the higher device gain at lower frequencies. This does require a degree of isolation from the driver stages to prevent the low frequency mismatch affecting the stability of these earlier stages. These networks are adequately covered in the literature (3, 4) and will not be further discussed here.

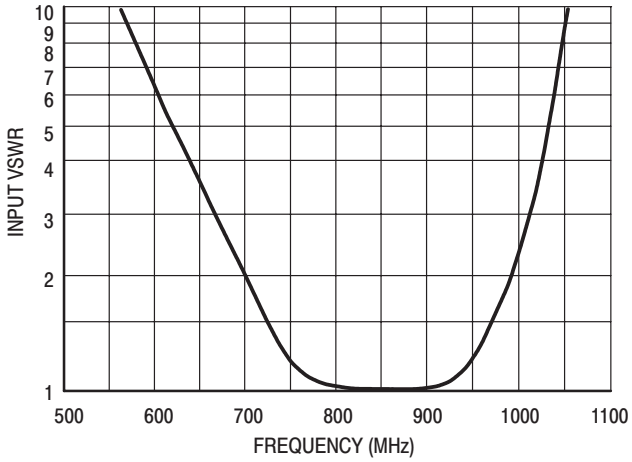

Figure 8. Input VSWR for Double Section Internal Match

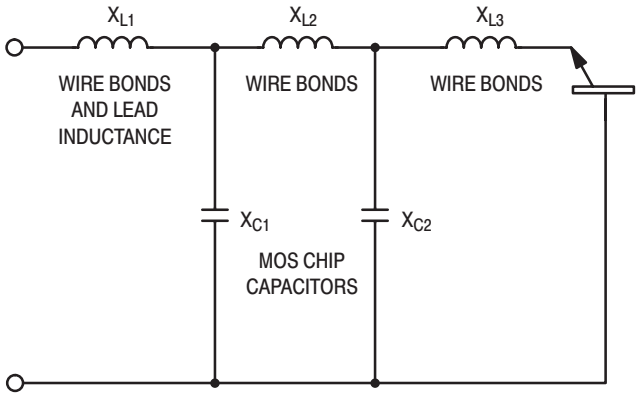

Figure 9. Double Section Input Matching

The input network transforms the die impedance up from 0.1 ohm to approximately the 8 ohm level. The inner section conforms closely to a typical internal match seen in existing products. The outer match requires relatively high values of inductance and, because of the common base configuration, also needs to carry the full emitter current with low loss. The minimum number of wires that can be used is therefore limited. The inductance is achieved by closely spacing the wires and using the mutual inductance to offset the lower self inductance of the many parallel wires.

Output Network

Reference to the transistor output model given in Figure 10 show the collector circuit can be represented by a parallel combination of shunt capacitance (C_c) and collector resistance (R_c) and the series collector lead inductance (L). Output impedance (Z_{out}) for this configuration is given by (8):

$$Z = \frac{R_s}{1 + (\omega_o C_c R_c)^2} + j\left[\omega L - \frac{(\omega R_c C_c)^2}{\omega C_c\,[1 + (\omega R_c C_c)^{2]}}\right] \quad (3)$$

If C_c is the dominant reactive term the intrinsic Q for the output network is given by:

$$Q = \omega R_c C_c \quad (4)$$

If the inductive term dominates which it normally does for high power transistors, then:

$$Q = \frac{\omega L}{R_c}\,[1 + (\omega R_c C_c)^2] \quad (5)$$

The maximum available output bandwidth becomes:

$$BW = \frac{f_o}{Q} = \frac{1}{2\pi R_c C_c} \quad (6)$$

if C dominates.

$$BW = \frac{R_c}{2\pi L[1 + (\omega R_c C_c)^2]} \quad (7)$$

if L dominates.

The value of collector resistance, R_c, can be calculated approximately, at high frequencies by:

$$R_c \approx \frac{1}{\omega_c C_c}$$

Therefore if L dominates:

$$BW = \frac{f_t}{LC_c\,(\omega_c{}^2 + \omega_o{}^2)} \quad (8)$$

$$= 106 \text{ MHz.}$$

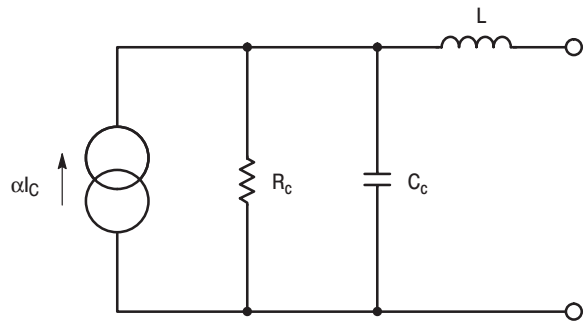

Figure 10. Transistor Output Model

This network could be conjugately matched for maximum power transfer but half of the power would be dissipated in the collector resistance limiting the maximum efficiency to 50%. Additionally, perfect matching will not necessarily allow the transistor to reach its full output power capability because of current saturation effects. The internal collector resistance for a class–C amplifier is also highly nonlinear and varies over a wide range as the transistor oscillates between saturation and cutoff during each RF cycle. In fact the shunt collector resistance is maximized during product development by the suitable selection of epitaxial resistivity and epitaxial thickness consistent with meeting the required collector breakdown voltages. High shunt collector resistance maximizes the efficiency and saturated power capability.

RF power transistors are normally operated with a collector load–line determined by assuming the maximum collector voltage swing during the device turn–off period will be twice the supply voltage. The load–line impedance can be approximated by the equation:

$$R_p = \frac{(V_{CC} - V_{CE(sat)})^2}{2 \times P_{out}} \quad (9)$$

This equation holds good for frequencies less than the cut–off frequency for the die (f_c). If we ignore the collector resistance (R_c) the matching problem simplifies to the collector capacitance shunted by R_p. Limitations of broadband matching for this load configuration have been analytically described by Bode (5).

We can apply Bode's resistance or attenuation integral theorem to estimate the available bandwidth for the transistor die neglecting the limitations of the package inductance:

$$\int_0^\infty R\,d\omega = \frac{\pi}{2C} \quad (10)$$

This expression applies to any minimum reactance network including a leading parallel capacitor where the source resistance can be considered substantially infinite. Capacitance is estimated to be 1.2 times Cobo. The multiplication factor was empirically determined by comparing measured impedance data with an optimized model of the die and the package parasitic elements and has been confirmed for a number of UHF and 800 MHz transistors. Using the modified capacitance value the constant resistance integral can be rewritten as:

$$\int_0^\infty R\,d\omega = 1.48 \times 10^{10} \text{ ohm.rad/s}$$

or

$$\int_{o}^{\infty} R\, d\omega = 2.36 \times 10^{9} \text{ ohm.hertz}$$

Analyzing the network shown in Figure 11 the series input resistance can be plotted for all frequencies (Figure 12). It is apparent from the graph that bandwidth is lost outside the frequency range we desire especially below 300 MHz.

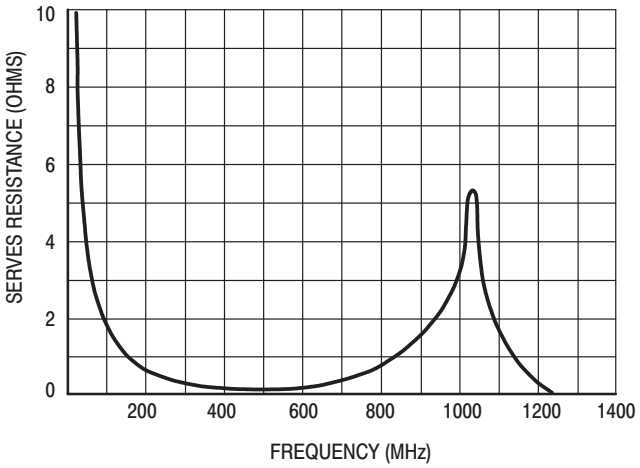

Figure 11. Series Resistance for Network at the Internal Collector Node

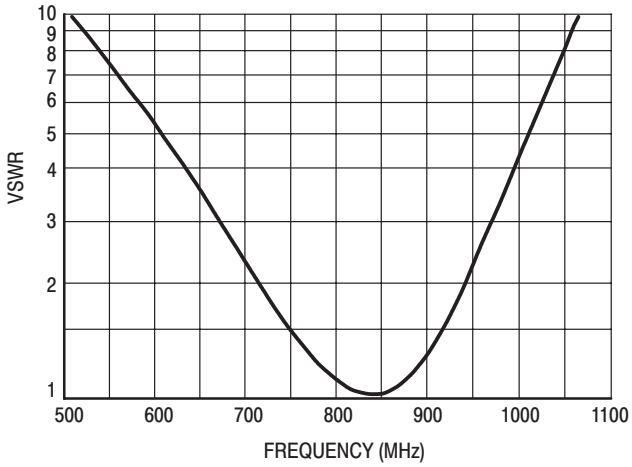

Figure 12. Bandwidth for Non–Internally Matched Output

If the area under the curve is integrated the result should correspond to the bandwidth–resistance product calculated from the resistance integral. It can readily be seen that by restricting the area under the curve to the operating frequency range and loading the internal collector node with the calculated load–line impedance the ultimate bandwidth is realized. At all frequencies outside the operating band, the series resistance seen by the internal collector terminal would need to be zero. The design of a network to match the available bandwidth would be impractical but typically only a fraction of the absolute bandwidth is normally required.

The above requirement on resistive behavior at the collector can be best met by adopting an ideal bandpass network that provides very abrupt transitions through zero resistance outside the operating range. Practical considerations, as in the case of the input network, limit the circuit topologies that can be incorporated inside the package. The un–matched case can be improved upon by some relatively simple internal changes to the package metallization which allow the die–bonding of an additional output MOS–capacitor.

Tuning out the collector–base capacitance at mid–band using a shunt–L element remarkably improves the usage of the available frequency–resistance product. This is clearly illustrated in Figure 13. The series resistance has been replotted for the new network shown in Figure 14. Maximum broadband power transfer is enhanced by this type of network but more important the impedance match is improved over the operating bandwidth. Efficiency, which has a greater sensitivity than gain to reactive loading at the internal collector node, does not suffer the roll–off at lower frequencies that would be seen with an un–matched design. Figure 15 is a comparative plot of normalized parallel reactance ($|X_p/R_p|$) for a shunt–L network and a conventional un–matched transistor. It can be seen that the shunt reactive component for the shunt–L match is higher at the low end of the band than in the case of the unmatched device. For a good match the reactance should be at least twice the parallel resistive component ($|X_p/R_p| > 2$) within the operating band (7).

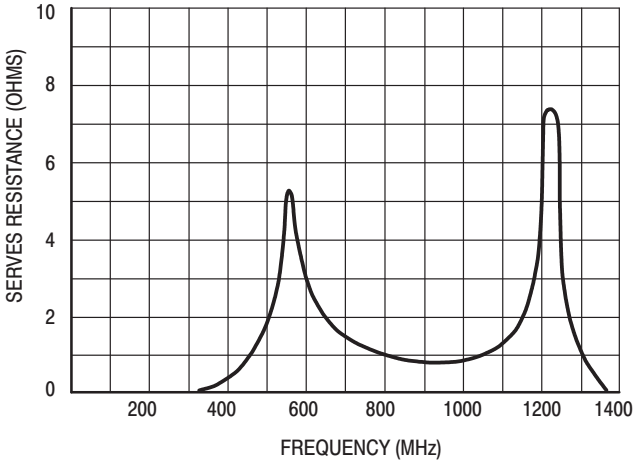

Figure 13. Series Resistance at Internal Collector Node for Output Network Including Shunt–L

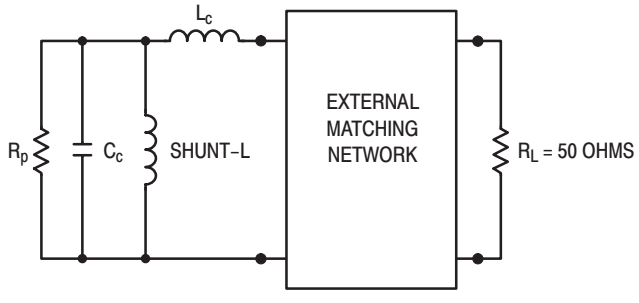

Figure 14. Collector Shunt–L Matching

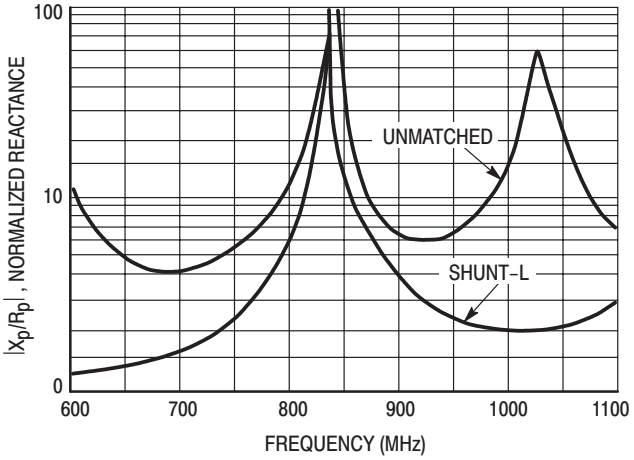

Figure 15. Normalized Reactance at Internal Collector Node for Output Matching Network

Again, as in the case of the input network an additional section of low–pass transformation can be included to further increase the impedances to a level which eliminates the need for an external shunt–C. Figure 16 shows the bandwidth attainable with the network shown in Figure 17.

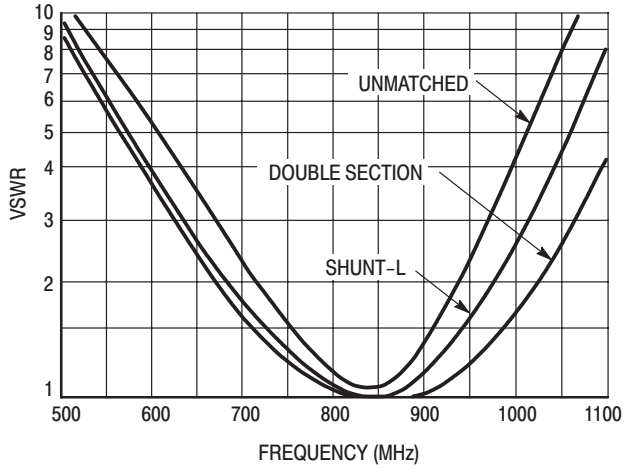

Figure 16. Improvement in Bandwidth with Output Matching

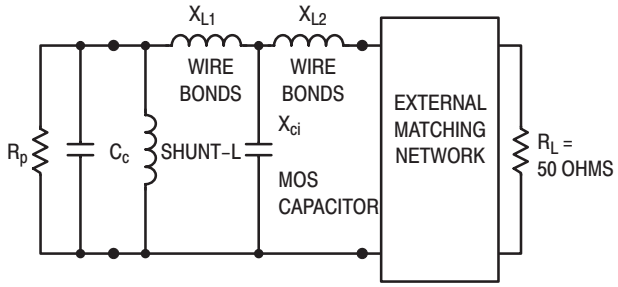

Figure 17. Double Section Collector Matching

External Matching Requirements

The high impedance levels present at the terminations of this package do greatly simplify the external matching requirements. The device can be matched to 50 ohms with a single section transmission line with a characteristic impedance in a range that can be readily fabricated. The circuit schematic (Figure 19) of the broadband fixture used for device evaluation illustrate the simplicity of the external matching. The elimination of the troublesome shunt capacitors close to the transistor package does simplify the production and enhance the consistency of the amplifier performance.

PERFORMANCE

The accompanying graphs illustrate the performance of the 24 Volt version of this device. Noteworthy is the flatness of the gain and efficiency response across the design bandwidth and the extension of this outside the normal frequency range of interest. The package size and higher efficiency result in the new transistor having a thermal resistance less than 1 Watt/°C.

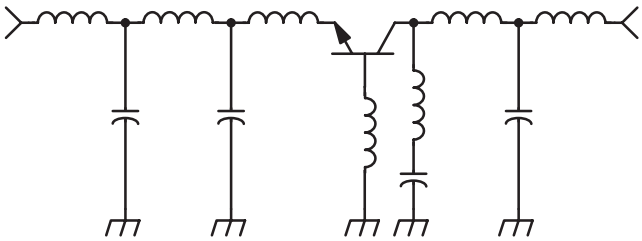

Figure 18. Simplified MRF898 Schematic Diagram

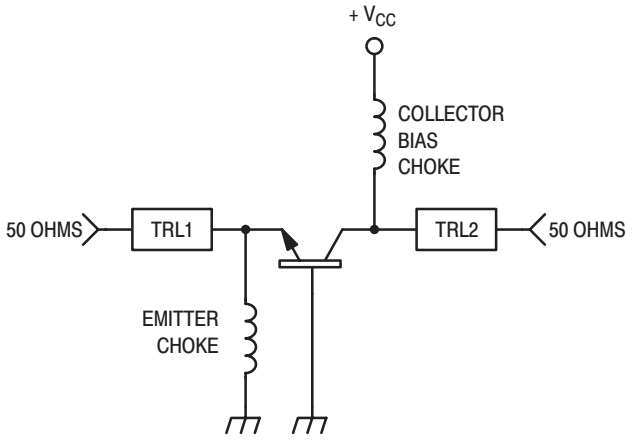

Figure 19. External Matching and dc Biasing

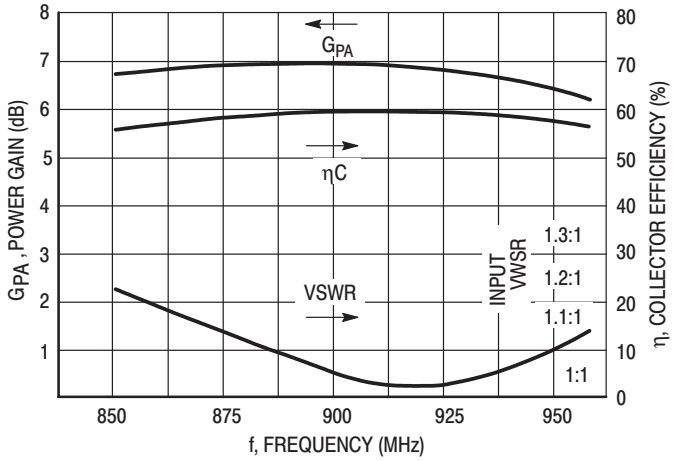

Figure 20. MRF898 Typical Broadband Circuit Performance

CONCLUSION

The design of RF power devices for high power, high frequency operation involves a number of compromises, most of which have been outlined above. The important points are that the added integration of additional matching inside the package can have the multiple benefits of easier usage, improved performance and better testability.

Conventional single input–matched parts will continue to be used at lower power levels but at higher power and higher frequency innovated product design is needed if devices are to be of practical value.

The package design outlined here offers several advantages over conventional 800 MHz packaging:

SIMPLER EXTERNAL MATCHING — Higher device impedances eliminate the need for critical shunt–C capacitors and allow single section transmission line matching.

HIGHER EFFICIENCY — High performance die and the use of shunt–L collector matching enable high efficiency ($>$ 60%) to be maintained over a greater bandwidth.

BETTER THERMAL PERFORMANCE — Larger package and higher operating efficiencies result in lower thermal resistance.

WIDER BANDWIDTH — Internal matching minimizes the effects of package parasitics allowing broader bandwidth and a minimum of variation in gain and efficiency across the operating band.

What of the future? Operation in excess of 100 Watts output power at 900 MHz has already been demonstrated with no changes required in the external matching. In fact this package concept can be extended to products operating at both higher and lower output powers than the examples given and the design is also feasible for products in the 400–512 MHz land mobile band.

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