A 17mW, 2.5GHz Fractional-N Frequency Synthesizer for CDMA-2000

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Outline

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Desired PLL Features for CDMA-2000

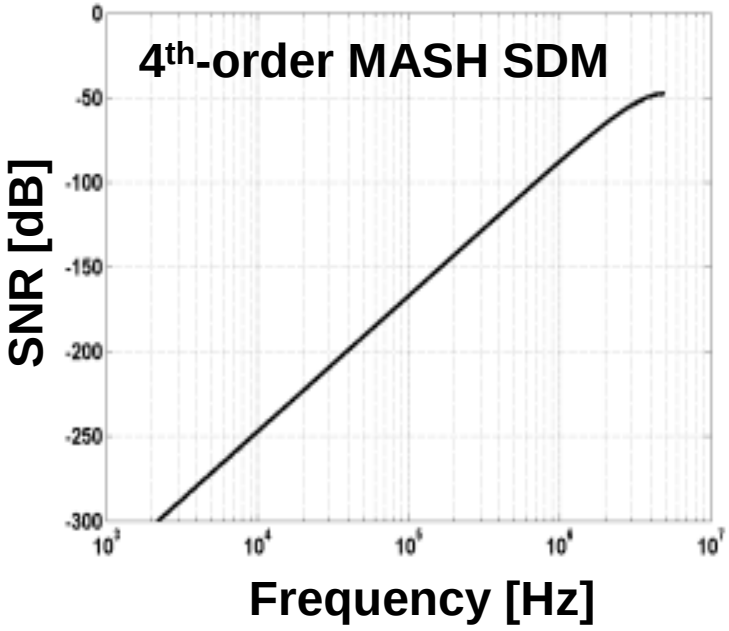
CDMA-2000 1x K-PCS	PLL requirements
144 kbps data transfer (2.5G)	Switching time < 500 μs ⇨ Loop bandwidth >10 kHz
Frequency Error <150 Hz	In-band pn <-75 dBc/Hz
Single-tone desensitization <-101 dBm @ 1.2 MHz	Out-of-band pn power < -135 dBc/Hz @1.2 MHz
LO freq. accuracy	10 kHz freq. Resolution
TX output power spectrum mask	<-60 dBc spurs

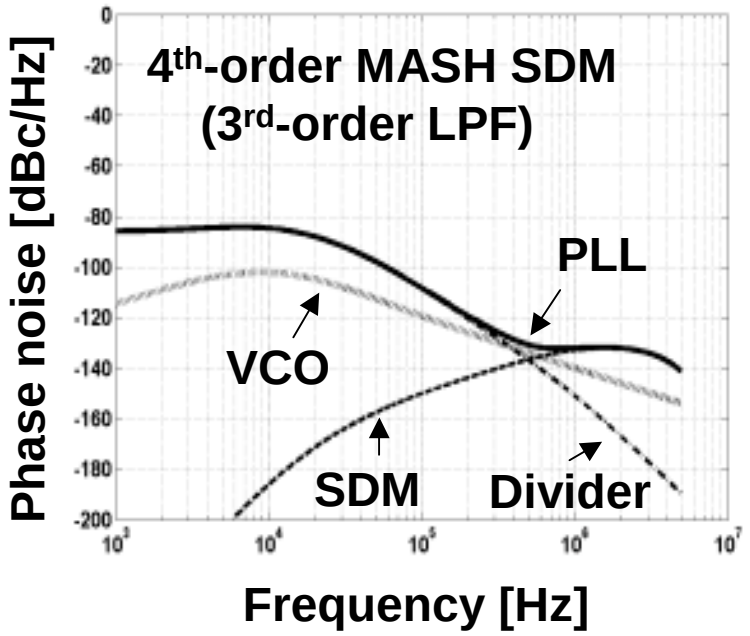
⇨ Conventional Integer-N: ***not a solution***

⇨ Fractional-N: ***a viable solution***

Design Issues in Fractional-N PLL using SDM

❶ Out-of-band phase noise boost around 1.0 MHz offset





❷ Fractional spurs

Multi-bit SDM FNPLL → a large fractional spur (-45 ~ -50dBc)
due to PLL nonlinearity
(Filiol-JSSC98, Rhee-ISSCC2000)

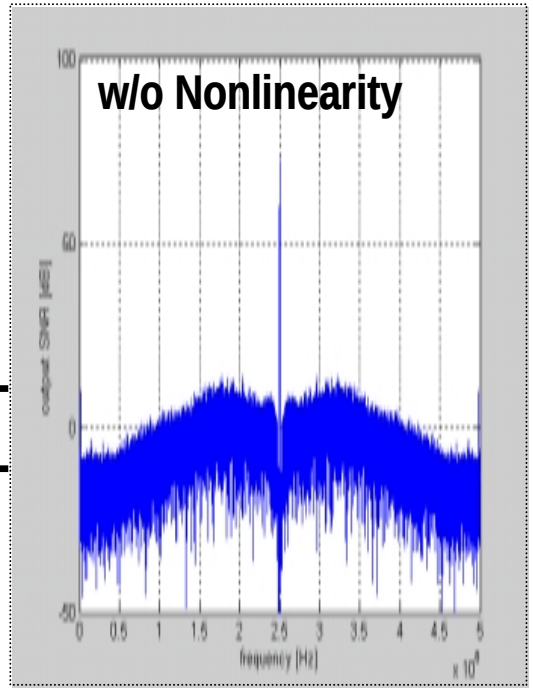
PLL Nonlinearity Effects

VCO output (60 kHz loop BW)

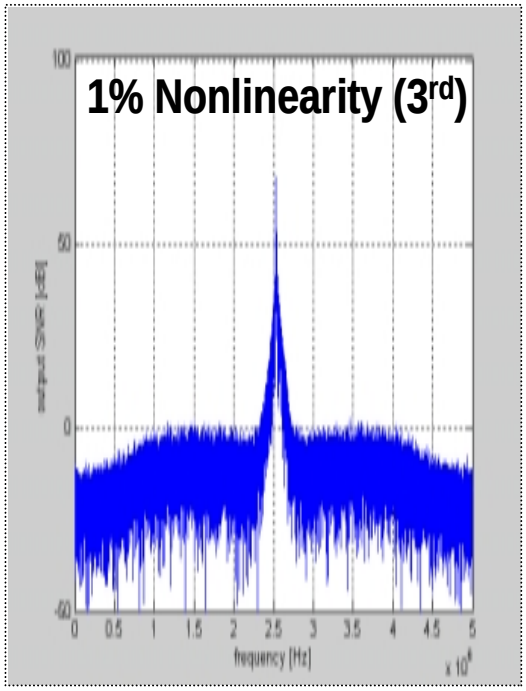
Multi-bit SDM (3-bit output)

Single-bit SDM (1-bit output)

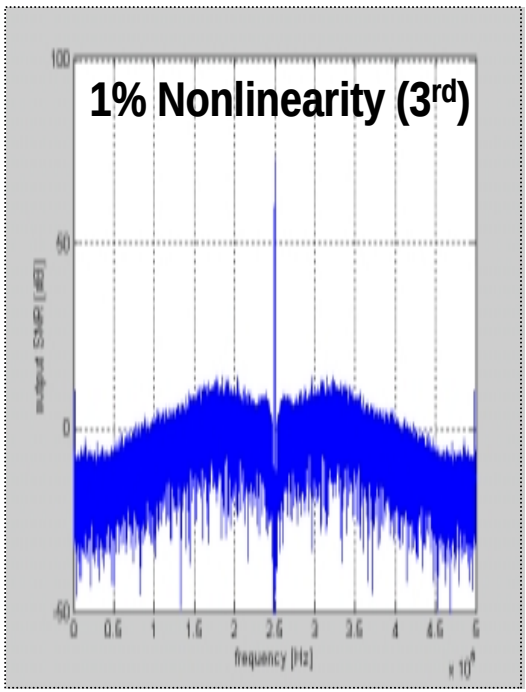
Output phase noise



Frequency



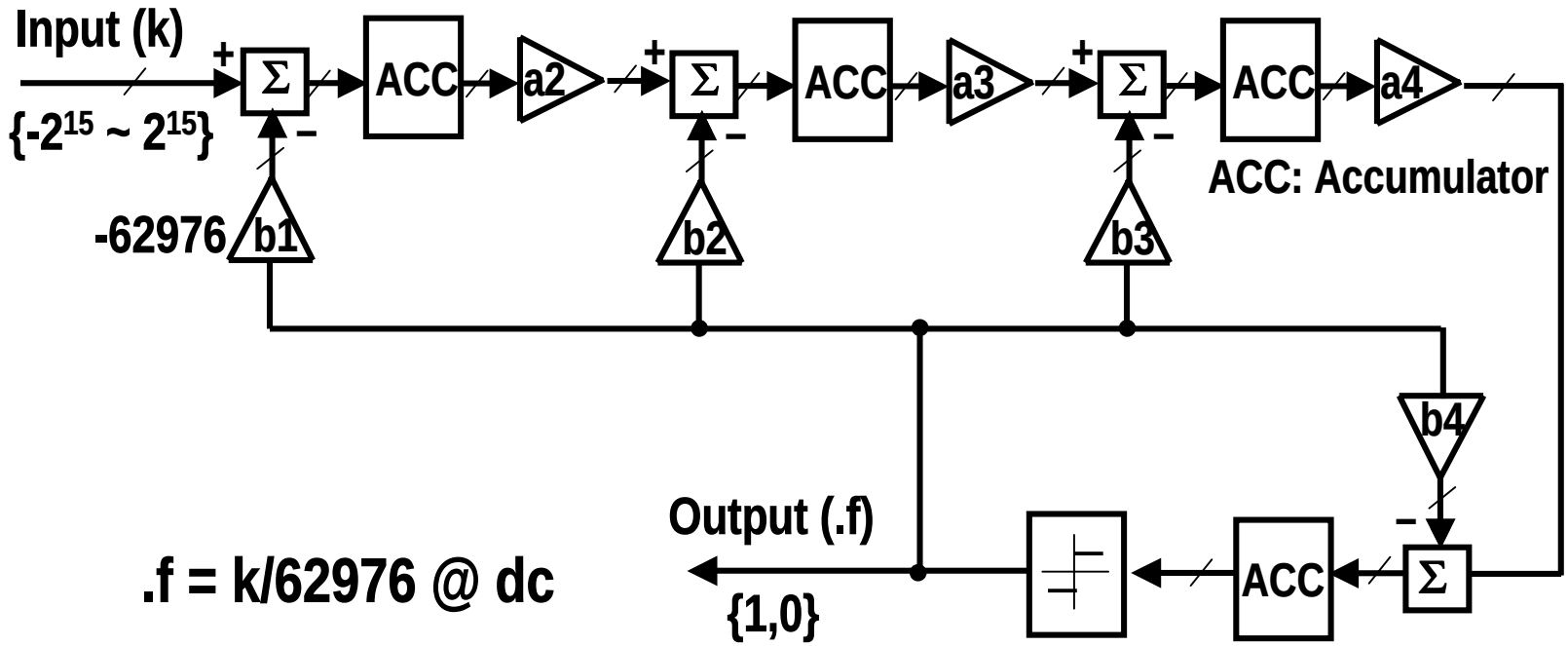
Frequency



Frequency

⇨ **Single-bit SDM free from PLL nonlinearities.**

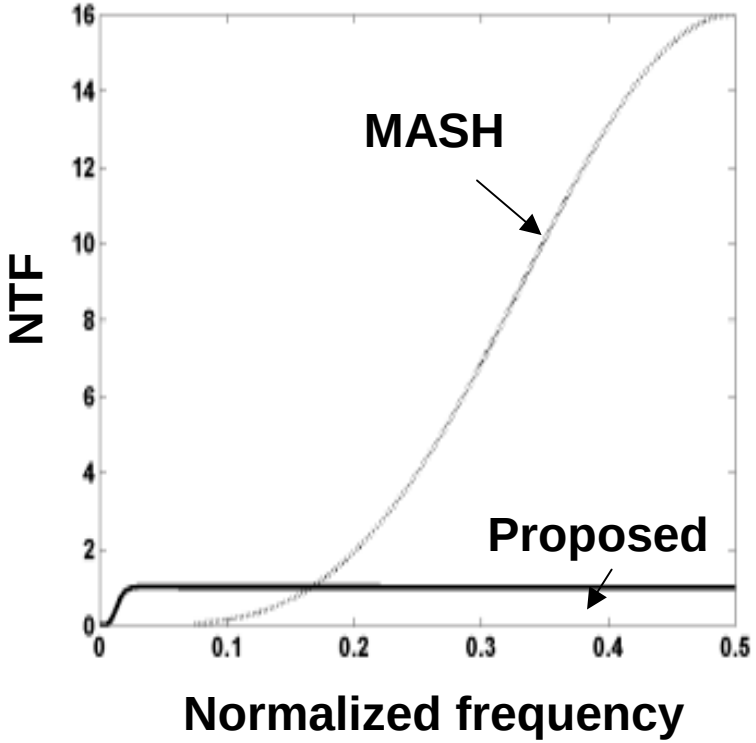
4^{th}-order 1-bit Digital SDM



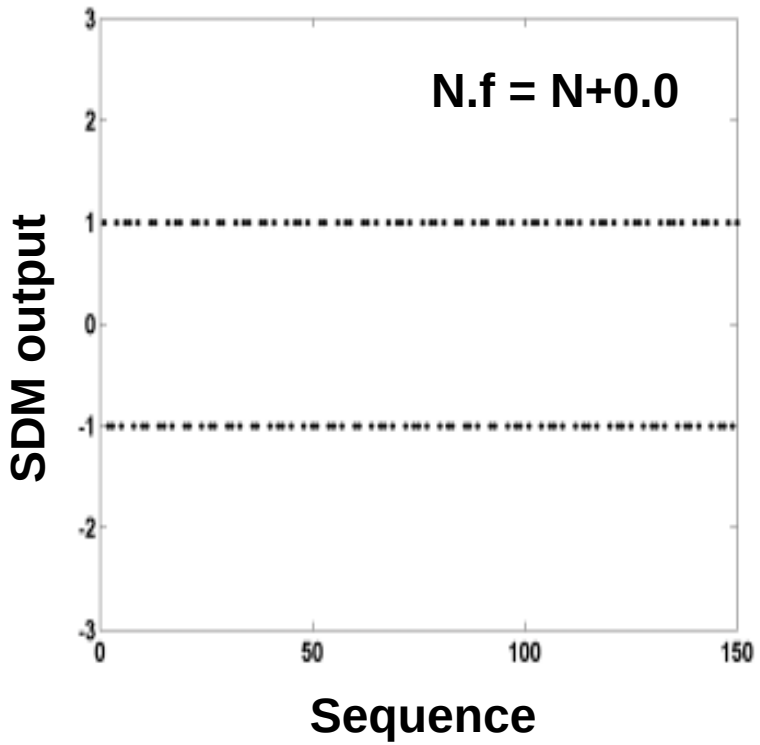
- $H_n(z) = (1 - z^{-1})^4 / D(z)$ where $D(z) = 1 + p_1z^{-1} + p_2z^{-2} + p_3z^{-3} + p_4z^{-4}$
- **Easy implementation of required 10 kHz resolution:**
  = 10 kHz/64 (= 9.84 MHz/62976)

Noise Performance of Proposed Modulator

Noise Transfer Function



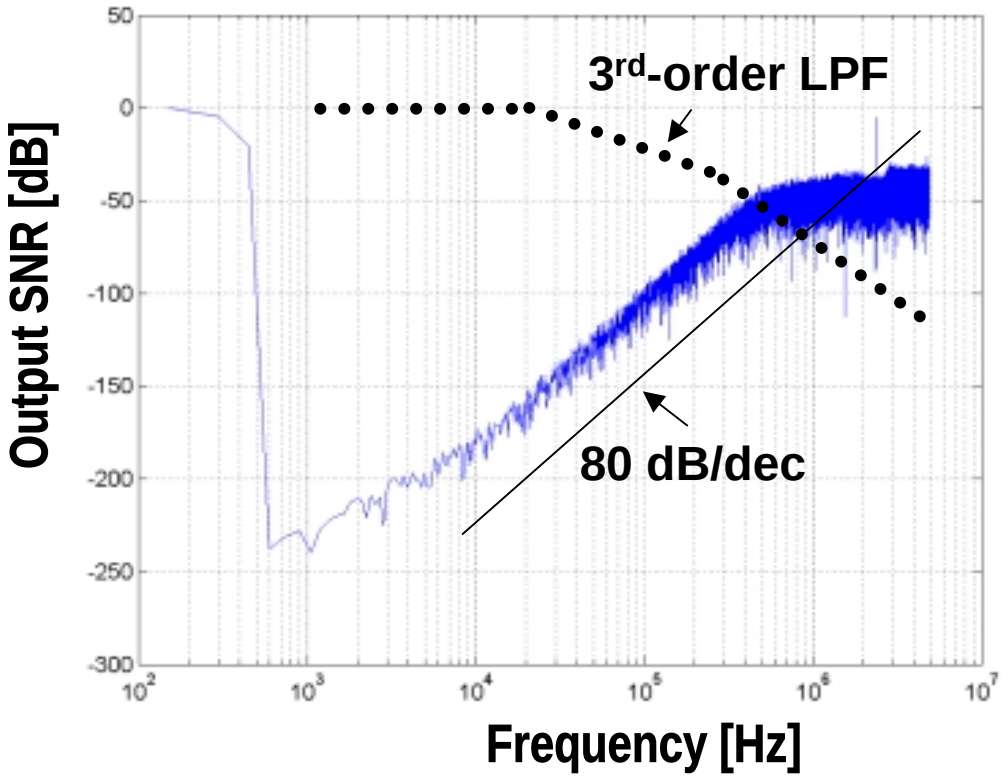
Output bit pattern



⇨ 16x smaller noise gain than MASH at 0.5* fs

⇨ Flat noise gain over bandwidth of 0.04* fs

Output SNR of Proposed Modulator

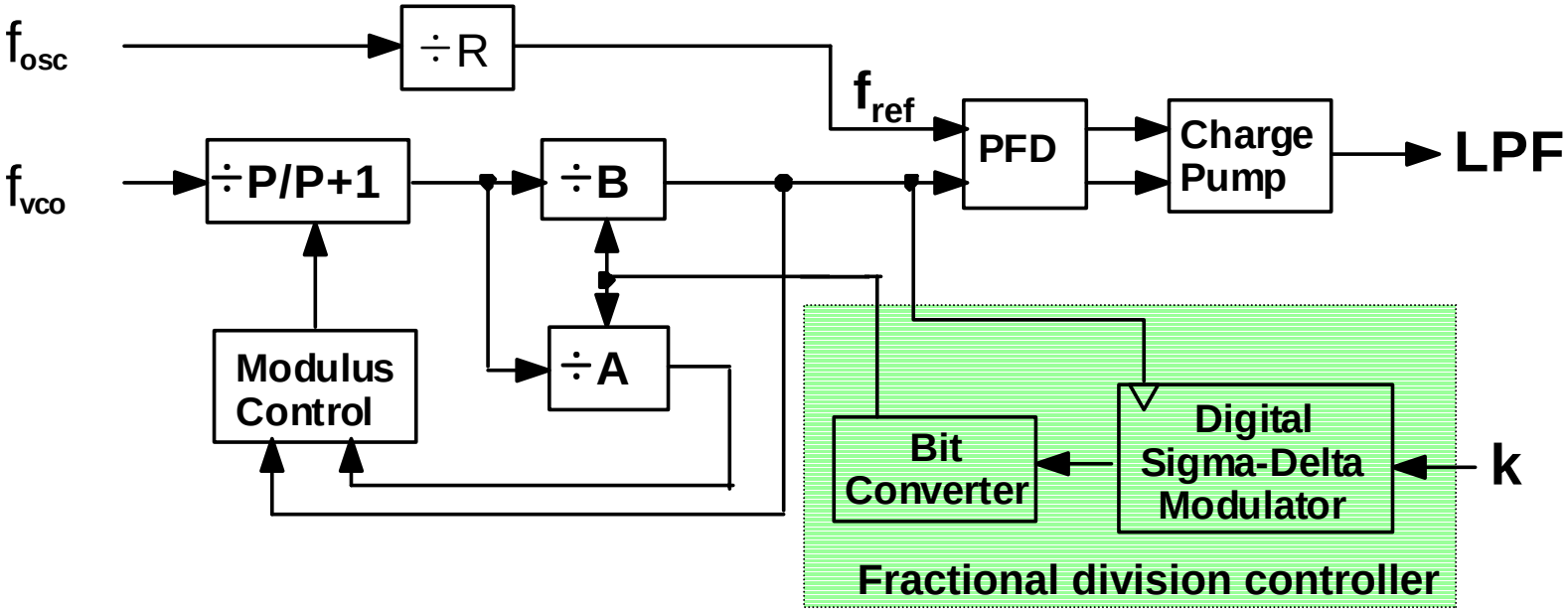


f_s = 9.84 MHz

N.f = N + 0.5

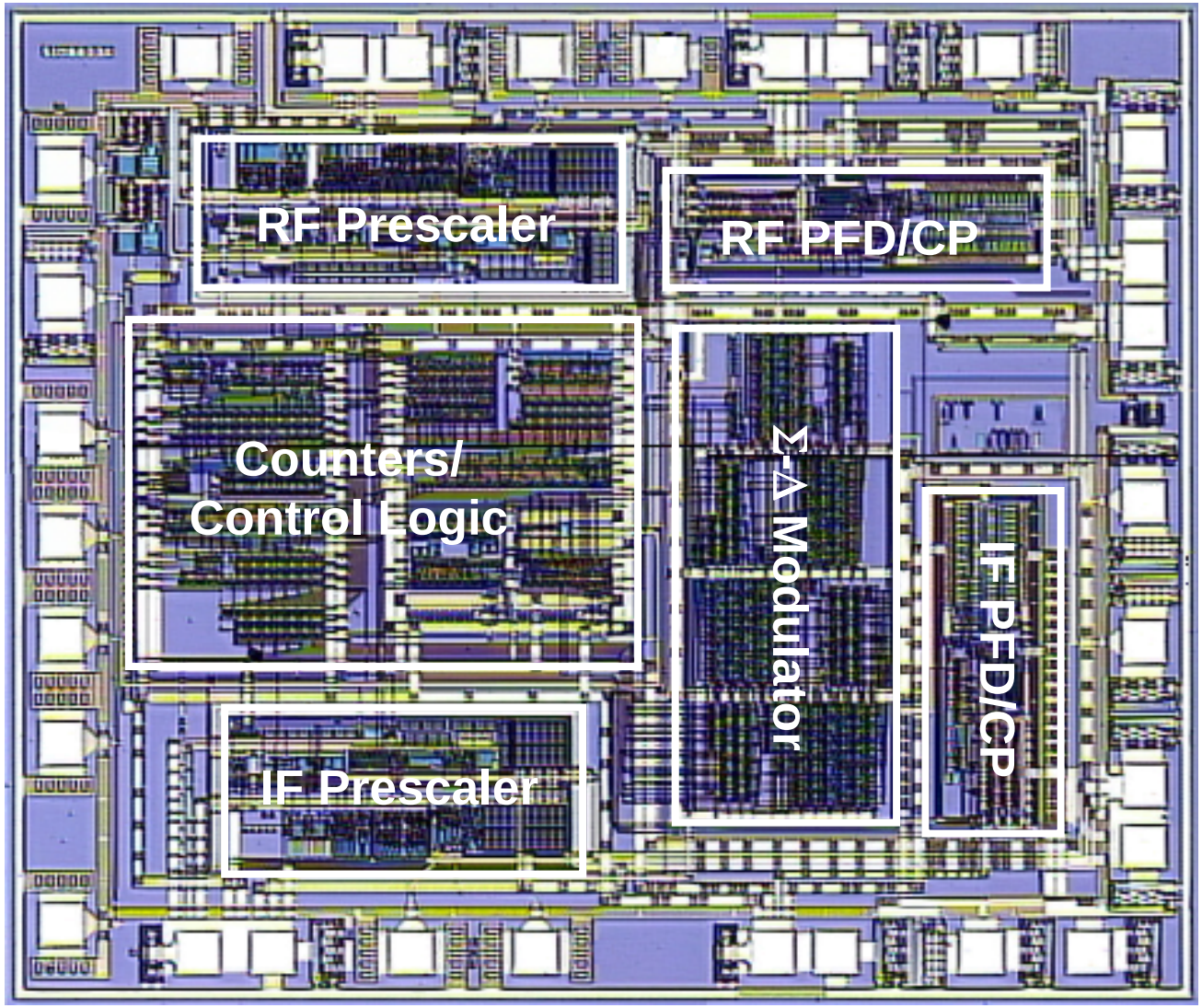
- Good performance with 4th-Order SDM

RF Fractional-N PLL Architecture



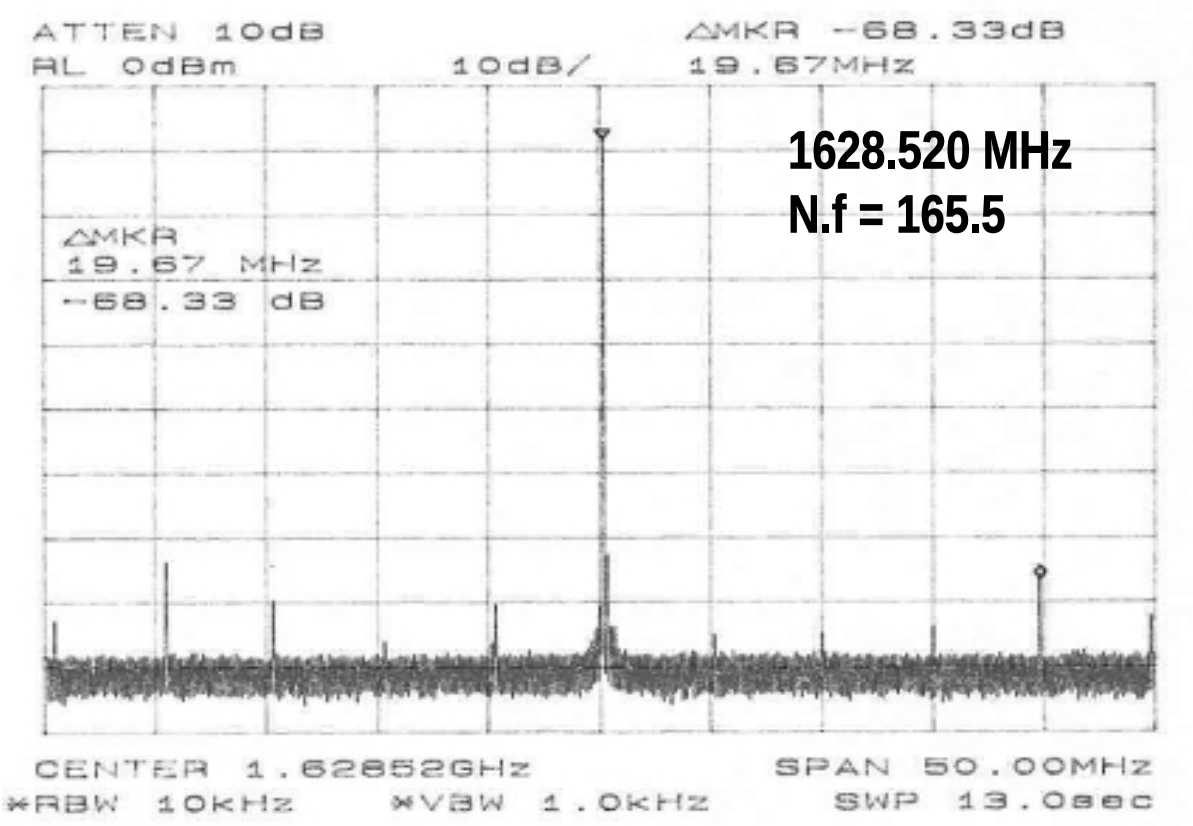
- **Simple Fractional-N Architecture**
  Pulse-swallowed dual-modulus divider + Single-bit 4th-order SDM
- **Low-Power Advantage**
  compared with other Fractional-N PLLs using multi-modulus divider
- **In lock state, $f_{vco} = N.f \bullet f_{ref} = (B \bullet P + A + k/62976) \bullet f_{ref}$**

Die Microphotograph



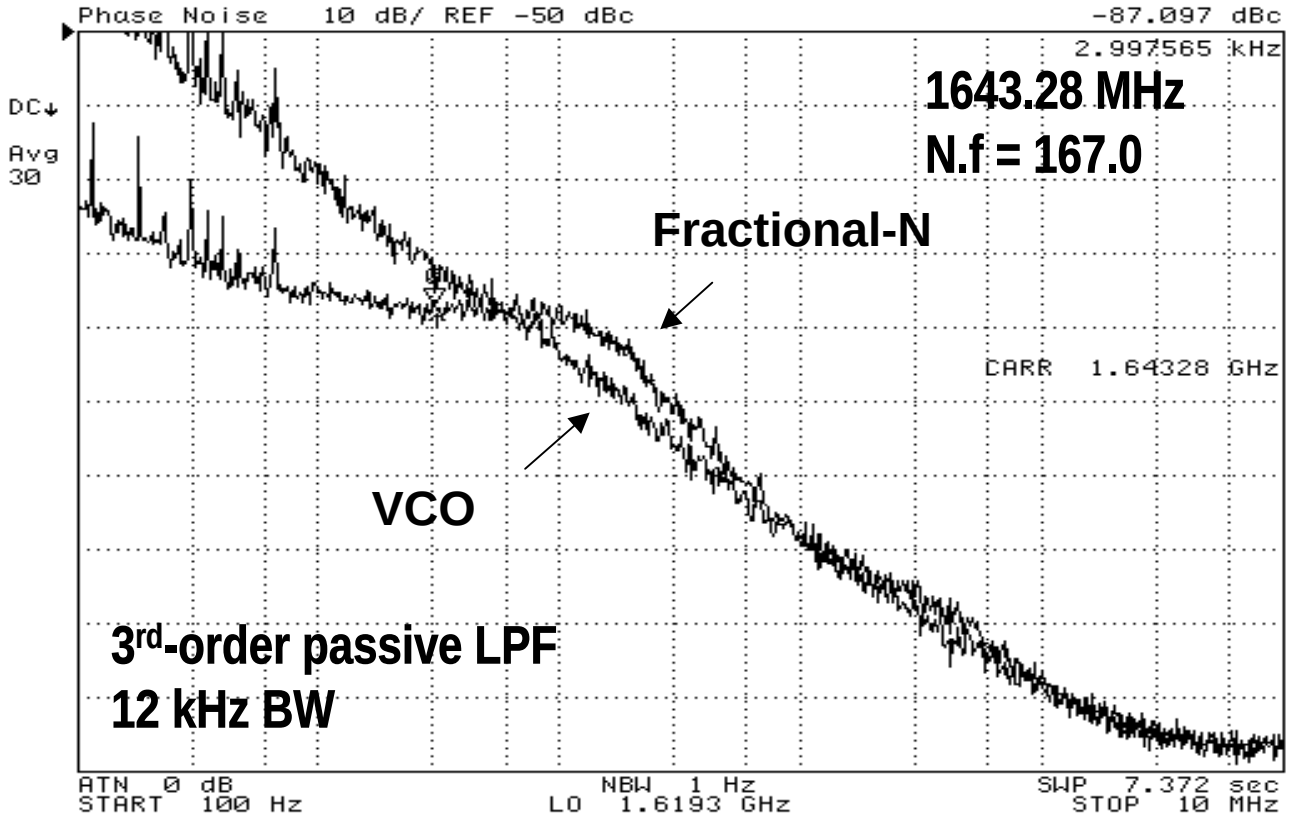
0.5μm -
BiCMOS
(15GHz f_t)

Measured PLL Output Spectrum



- Reference Spur: -68 dBc @ 19.68 MHz (= f_{osc})

Measured PLL Phase Noise



- SSB Phase Noise ~ -87 dBc/Hz @ in-band
  -139 dBc/Hz @ 1 MHz offset

Measured Performance

Supply Voltage (V_{dd})	2.7–4.0 V
Current consumption	
RF / (RF+IF)	5.5 mA / 7.0 mA @ 3.0V V_{dd}
Power save mode	< 1 μA
Max. operating frequency	> 2.5 GHz
RF input sensitivity	< –15 dBm
Phase noise	–87 dBc/Hz @ in band
	–139 dBc/Hz at 1.2 MHz
Reference spurs	< –68 dBc
Fractional spurs	< –85 dBc
Switching time	< 500 μs (30MHz step)

Conclusions

- A 2.5 GHz fractional-N frequency synthesizer is presented with single-bit 4^{th}-order SDM and pulse-swallowed dual-modulus divider, in 0.5 μm BiCMOS.

- Single-bit SDM less sensitive to PLL nonlinearities.

- Measured performance meets CDMA-2000 1x requirements.
  - Channel switching time < 500 μs, in-band phase noise: -87 dBc/Hz
  - Out-of-band phase noise: -139 dBc/Hz at 1.2 MHz