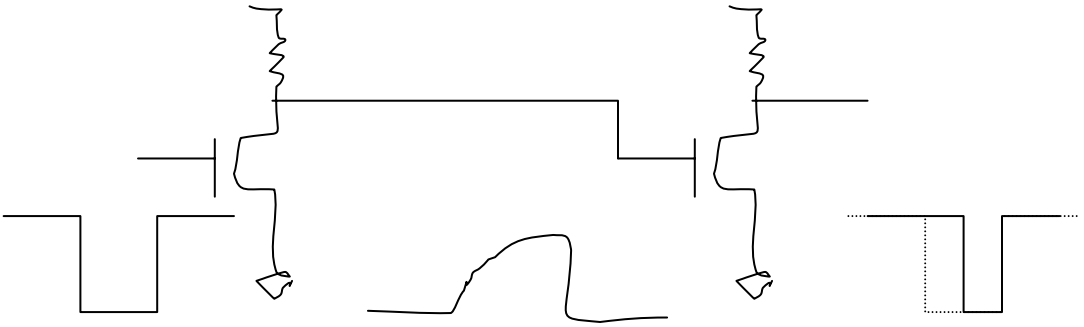
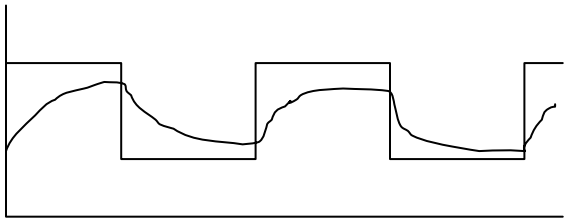
6.002 Demo#11, 11A, 11B (Load Set up demo#11.set): (Load Set up demo#11A.set): (Load Set up demo#11B.set)
Gate Delay **Agarwal Fall 00**
Lectures 12 and 13

Purpose: This demo examines gate delay using two cascaded MOSFET inverters, and also an RC circuit model. A square-wave input is applied to the first inverter, and the three relevant waveforms (input, middle, output) are shown on the scope. By increasing the frequency of the input, the gate delay becomes more pronounced (relative to the square wave period). The middle waveform exhibits the usual decaying exponential response, resulting in a delayed reaction by the second inverter.
The second portion of this demo shows the response of an RC (LPF) circuit to a square wave input. This is used to motivate and justify the gate-to-source capacitance model of the MOSFET.

Steps:
1. With the square-wave input to the cascaded inverters set to a low frequency (100 Hz), observe the input, the middle waveform (between the two inverters) and the output on the scope. Note that the signals are all consistent with the S or SR models of the MOSFET.
2. With the square-wave input set to a higher frequency (3 kHz), observe again the three waveforms on the scope. Note the slow rise of the middle waveform, and the corresponding delay in the output transition (and the subsequent change in duty cycle).
3. Switch to the RC circuit driven by a square-wave input. Note the decaying-exponential response. This motivates the gate-to-source capacitance model for the MOSFET. (Note: it might be desirable to show the capacitor current using the voltage across the resistor.)
4.



Input Slow-rise middle waveform delayed ouput



Square wave and RC circuit output

Description: Gate Delay

1) First set FG1 @ 100 HZ square wave, Amplitude @ 5 v p-p, offset @ 2.5 v p-p , observe the 3 waveforms @ CH1, CH2 and CH3 and see no delays.
2) Change frequency (FG1) from 100 HZ to 3 KHZ, amplitude and offset remain the same. Go to load setup and load Demo #11A, observe the 3 waveforms again @ CH1, CH2 and CH3 and see the delays.
3) Change the switch on the board to RC CKT set FG2 frequency @ 1 KHZ square wave, Amplitude @ 5 v p-p, offset @ 2.5 v p-p. Go to load setup and load Demo # 11B, observe CH1 and CH4 waveforms.

Note: FG1 and FG2 should be set @ HiZ!
See schematic diagrams and waveforms on the next for more info and pins out!!
Also see Fg1 and Fg2 on the next page.
This demo we use power supply to charge the capacitor and discharge it thru a bulb…

Oscilloscope Setup

CH	V/DIV	OFFSET	MODE	FUNC	MATH	VERTICAL	HORIZONTAL
1 on	5	-10.57	DC	off			
2 on	5	4.78	DC	off			
3 on	5	15.4	DC	off			
4 off				off			

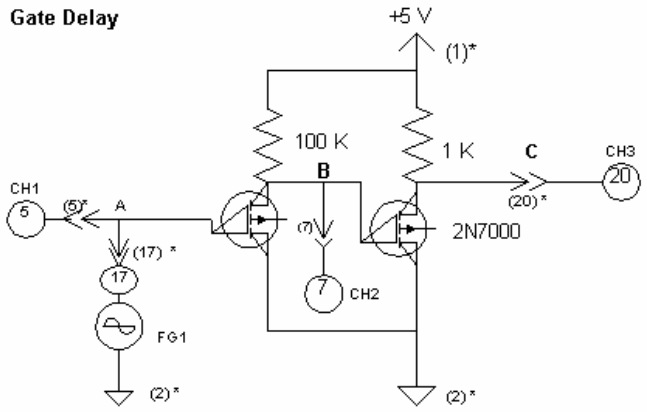
Horizontal: 1 m **Acquisition:** **Trigger: CH4**

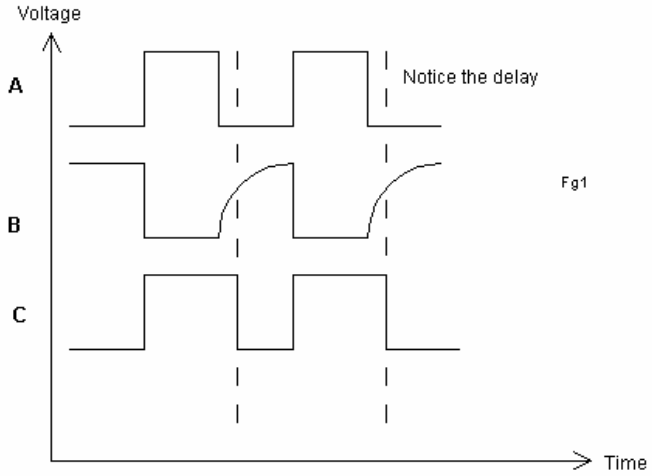
Waveform Generator Setup **Power Supply Setup**

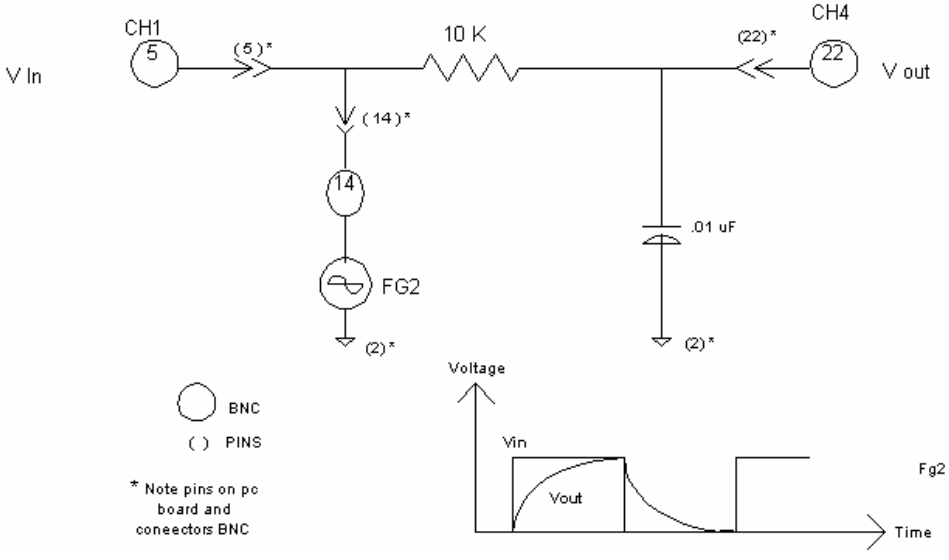
UNIT	WAVE	AMP	OFFSET	FREQ	+6	+25	-25	OUTPUT
FG1	Square	5	2.5	500 HZ	0	5	0	on
FG2	Square	5	2.5	1 KHZ			Trigger:	INT

Note: For Prof. Agarwal load Demo#11AA.set also he changed FG1 freq to 500 HZ
Note: Demo#11C to show only input and output gate waveform is hidden, but can be Ckicked to show .

Gate Delay


+5 V
(1)*
100 K
1 K
B
C
CH3
20
CH1
5
(5)*
A
(20)*
(7)
2N7000
(17) *
17
7
CH2
FG1
(2)*
(2)*


Voltage
A
Notice the delay
Fg1
B
C
Time


CH1
5
(5)*
10 K
(22)*
CH4
22
V In
V out
(14)*
14
.01 uF
FG2
(2)*
(2)*
BNC
( ) PINS
* Note pins on pc board and coneectors BNC
Voltage
Vin
Vout
Fg2
Time