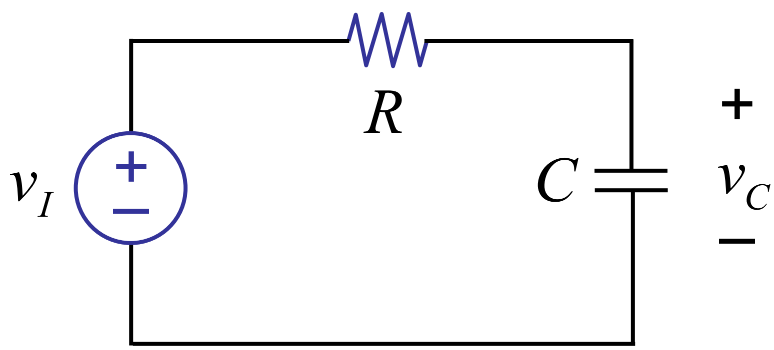
State and Memory

Review

Recall



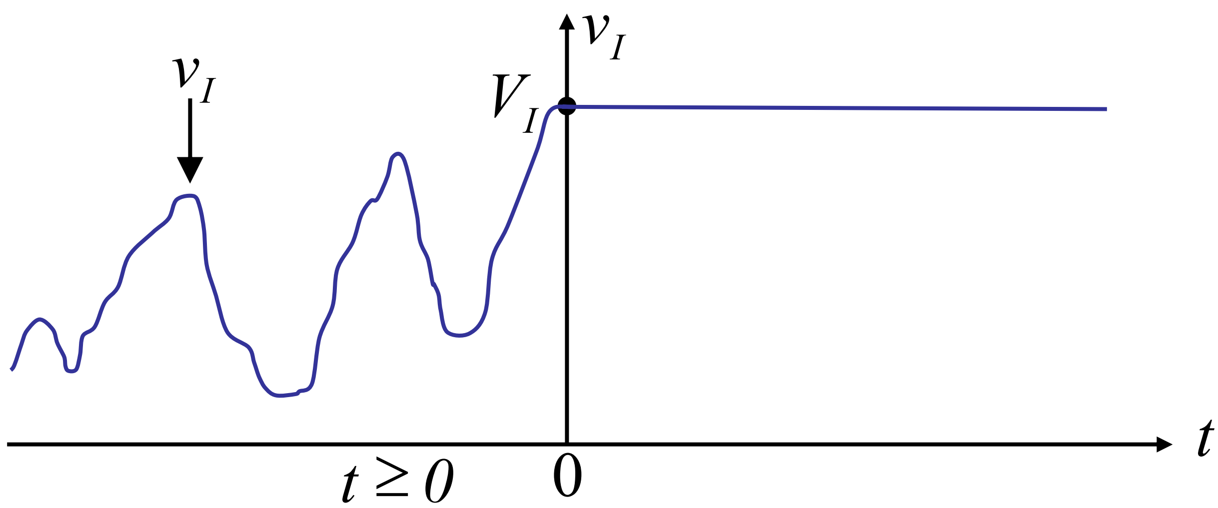
$v_I = V_I$ for $t \geq 0$ $\qquad v_C(0)$

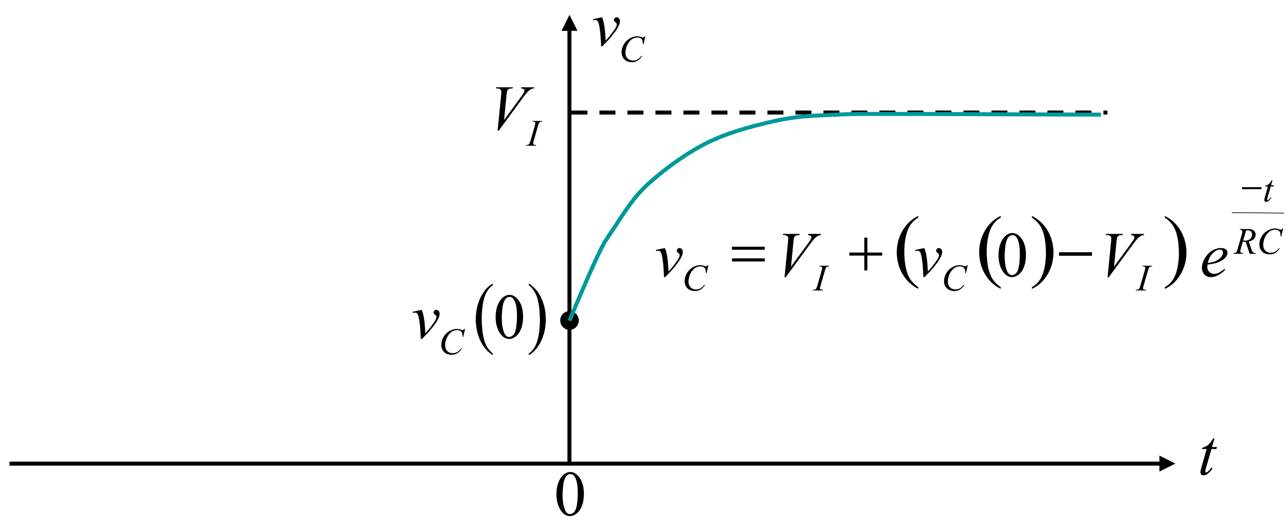
$$v_C = V_I + \left(v_C(0) - V_I\right) e^{\frac{-t}{RC}} \quad \text{—} \quad 1$$

Reading: Sections 10.3, 10.5, and 10.7

This lecture will dwell on the memory property of capacitors.

For the RC circuit in the previous slide





Notice that the capacitor voltage for $t \geq 0$ is independent of the form of the input voltage before $t = 0$. Instead, it depends only on the capacitor voltage at $t = 0$, and the input voltage for $t \geq 0$.

State

State : summary of past inputs relevant to predicting the future

$$q = C\,V$$

for linear capacitors, capacitor voltage V is also state variable

state variable, actually

State

Back to our simple RC circuit 1

$$v_C = f(v_C(0), v_I(t))$$

$$v_C = V_I + (v_C(0) - V_I)\, e^{\frac{-t}{RC}}$$

Summarizes the past input relevant
to predicting future behavior

State

We are often interested in circuit response for

- zero state $\quad v_C(0) = 0$
- zero input $\quad v_I(t) = 0$

Correspondingly,

- zero state response or *ZSR*

$$v_C = V_I - V_I\, e^{\frac{-t}{RC}} \qquad \text{———} \quad (2)$$

- zero input response or *ZIR*

$$v_C = v_C(0) e^{\frac{-t}{RC}} \qquad \text{———} \quad (3)$$

One application of STATE

↓

DIGITAL MEMORY

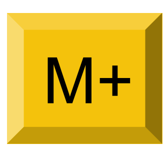
Why memory?

Or, why is combinational logic insufficient?

Examples

- Consider adding 6 numbers on your calculator

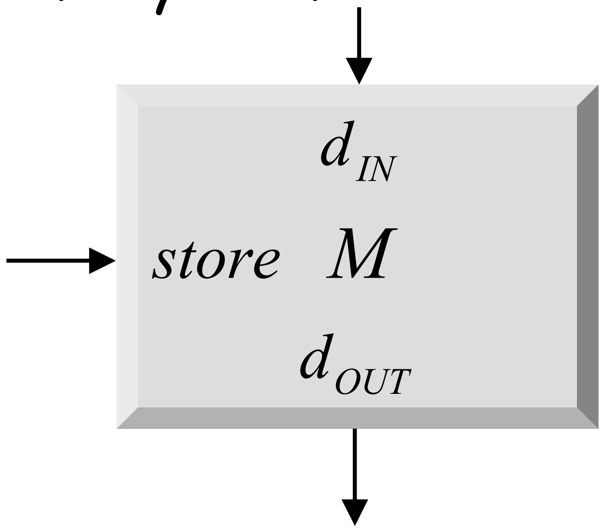
  2 + 9 + 6 + 5 + 3 + 8

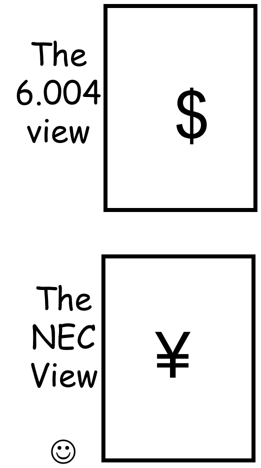


- "Remembering" transient inputs

Memory Abstraction

A 1-bit memory element

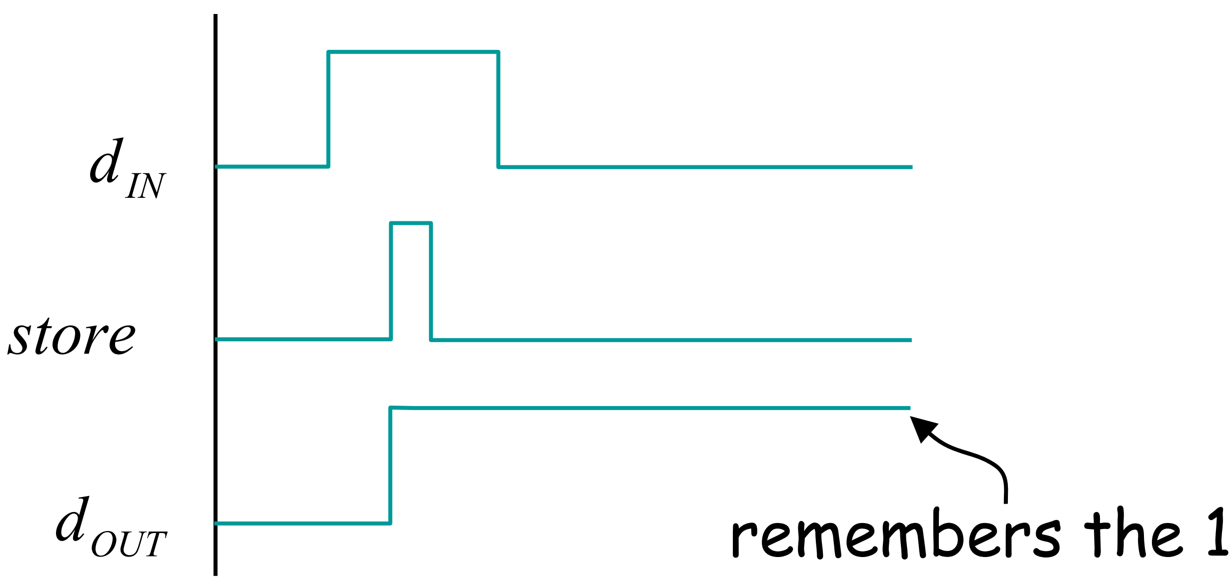




Remembers input when *store* goes high.

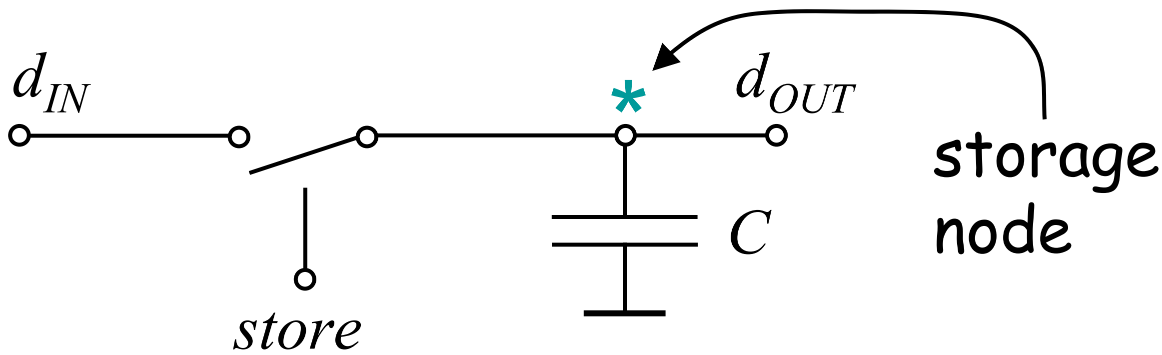
Like a camera that records input (d_{IN}) when the user presses the shutter release button.

The recorded value is visible at d_{OUT}.



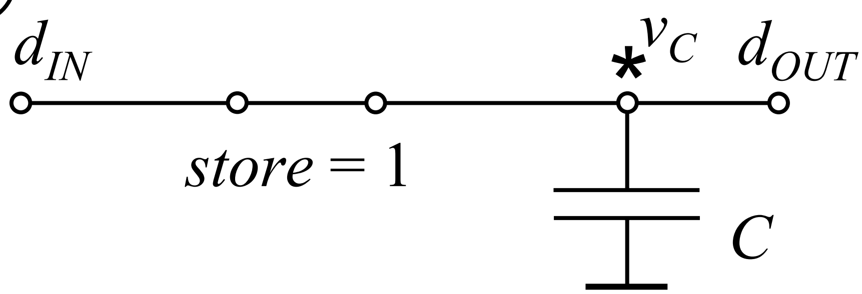
Building a memory element …

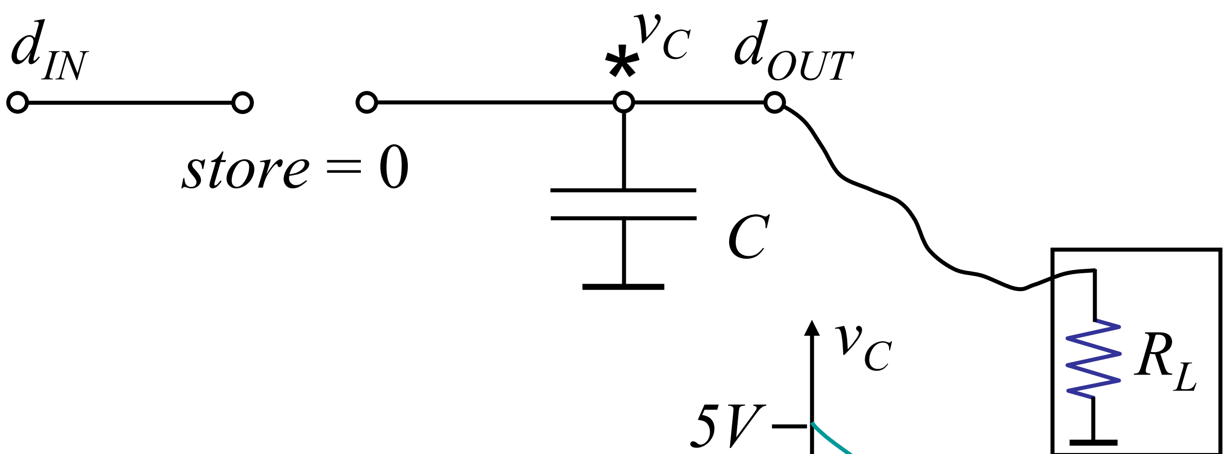
Ⓐ First attempt



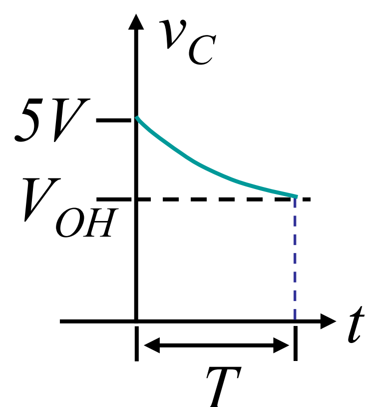
Building a memory element ...

A





Stored value leaks away



$$v_C = 5 \cdot e^{\frac{-t}{R_L C}}$$

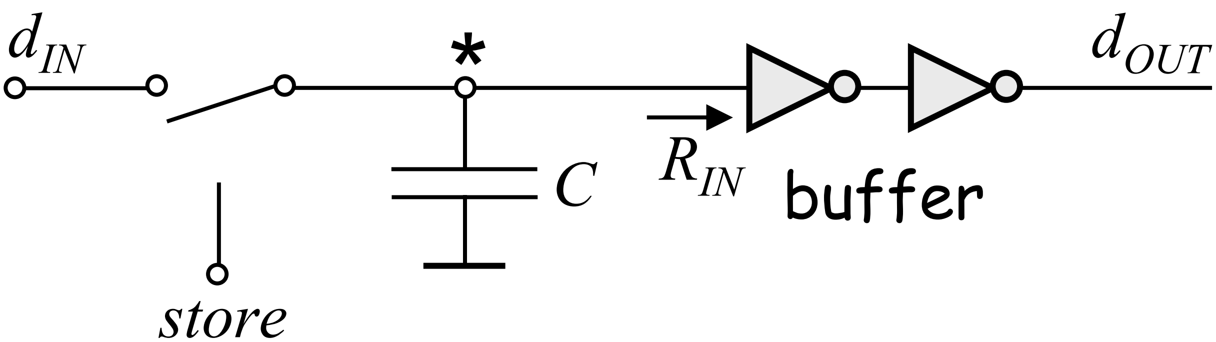
from 2

$$T = -R_L C \ln \frac{V_{OH}}{5}$$

store pulse width >> $R_{ON}\ C$

Building a memory element …

Ⓑ Second attempt → buffer



Input resistance R_{IN}

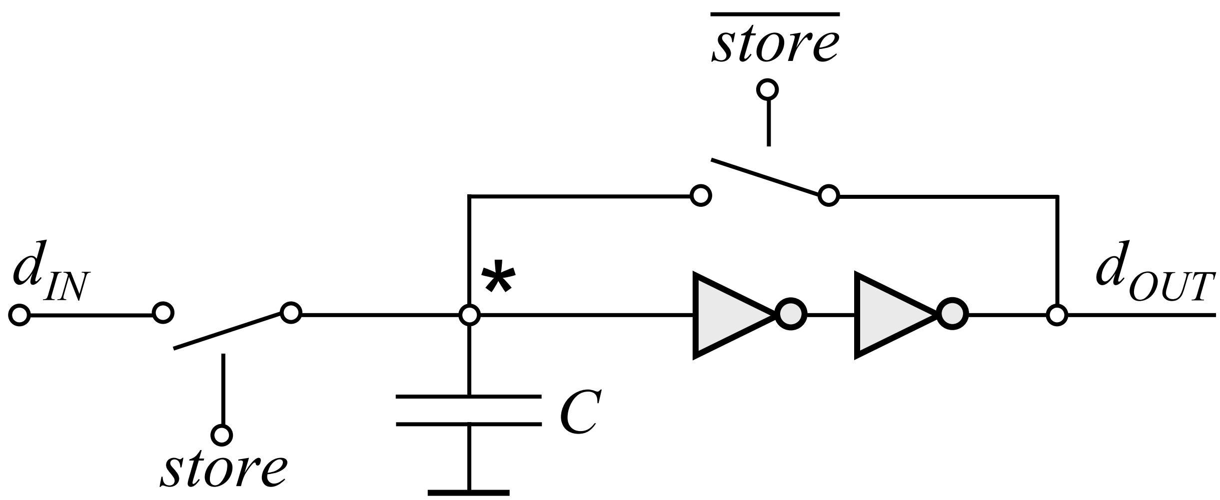
$$T = -R_{IN} C \ln \frac{V_{OH}}{5}$$

$$R_{IN} >> R_L$$

Better, but still not perfect.

Building a memory element …

Ⓒ Third attempt → buffer + refresh

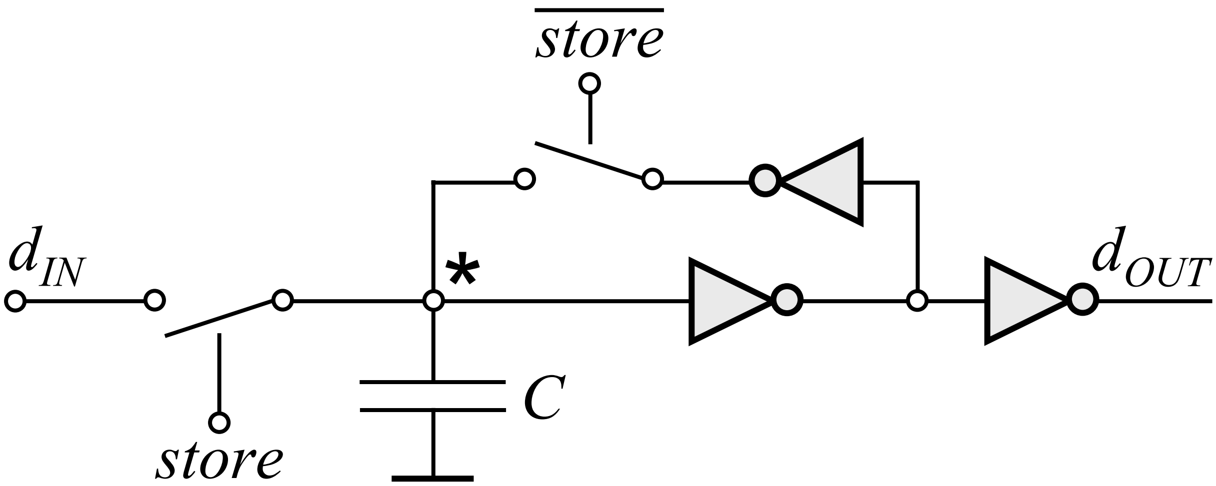


Does this work?

No. External value can influence storage node.

Building a memory element ...

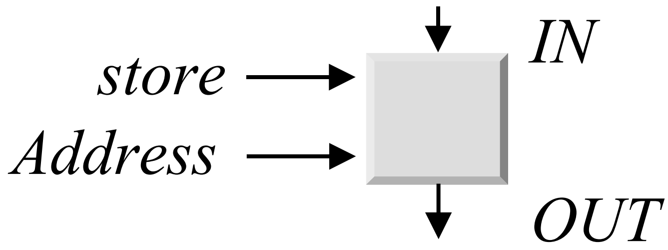
Ⓓ Fourth attempt → buffer + decoupled refresh

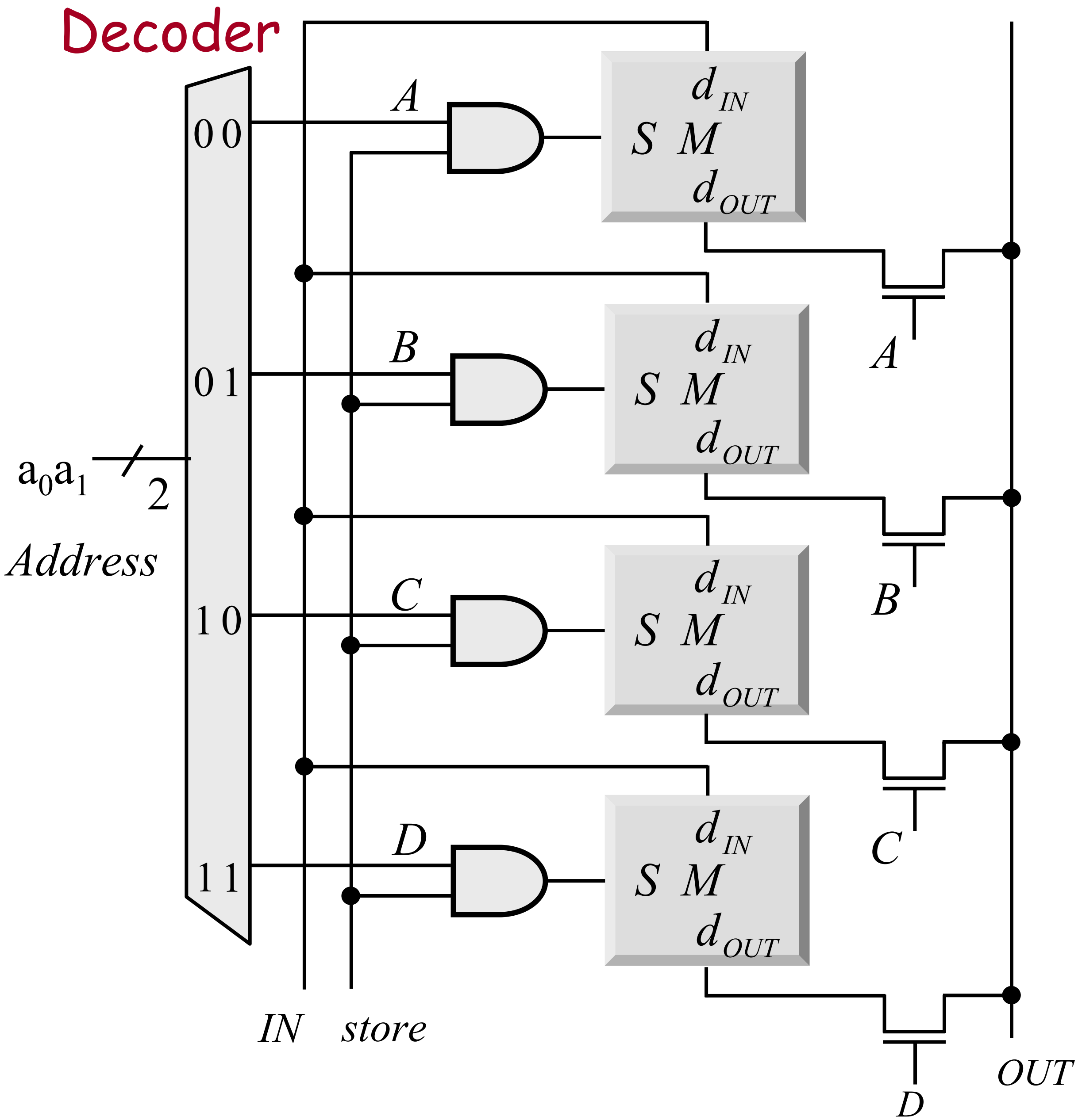


Works!

A Memory Array

4-bit memory





Truth table for decoder

a_0	a_1	A	B	C	D
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Agarwal's top 10 list on memory

10 I have no recollection, Senator.
9 I forgot the homework was due today.
8 Adlibbing ≡ ZSR
7 I think, therefore I am.
6 I think that was right.
5 I forgot the rest …